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# MS-7887

## Intel -SharkBay plamform Z87

MIN ITX

Ver: 1.0(17x17)

CPU:

System Chipset:

Haswell LGA1150

Lynx Point Z87

Onboard Chip:

HD Audio Codec:ALC1150

LAN-Atheros E2205-B

SIO:Nuvoton 6779D

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) \* 2 (Dual Channel)

ACPI:

PWM:

UPI

UP1649 6 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot \* 1

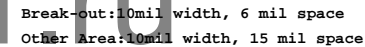
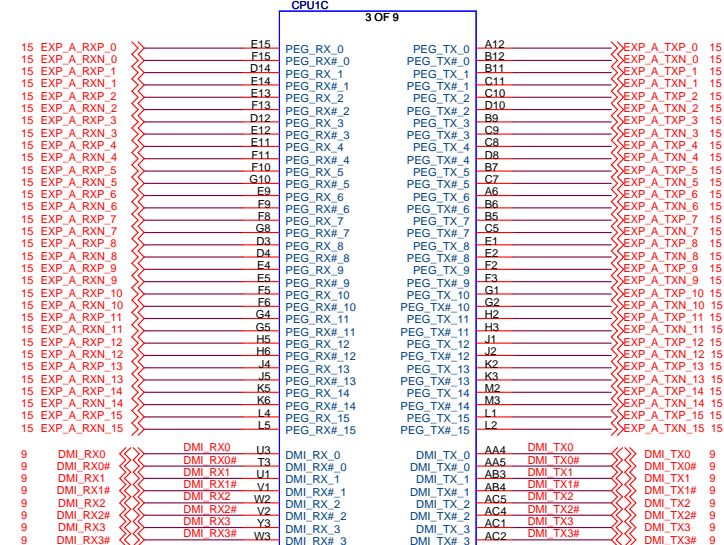
SATA3.0 x5(PCH)  
ESATA x1(PCH)  
REAL USB2.0 \*2  
FRONT USB2.0 \*2  
REAL USB3.0 \*4  
FRONT USB3.0 \*2

MS-7851 Block Diagram

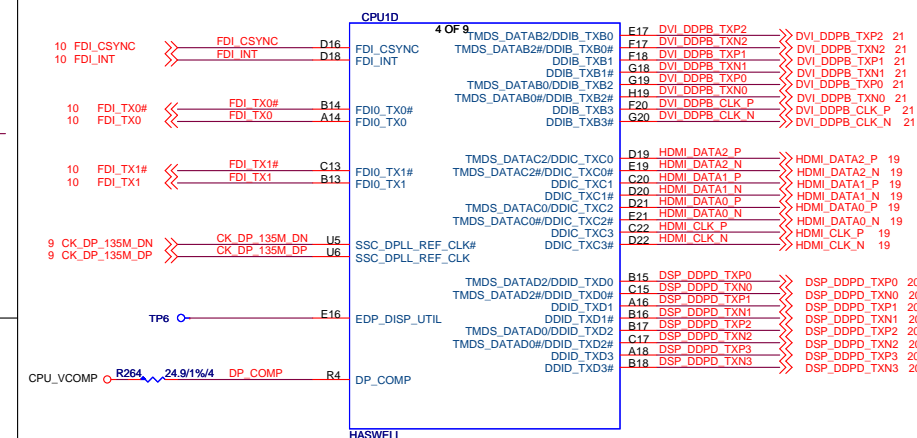
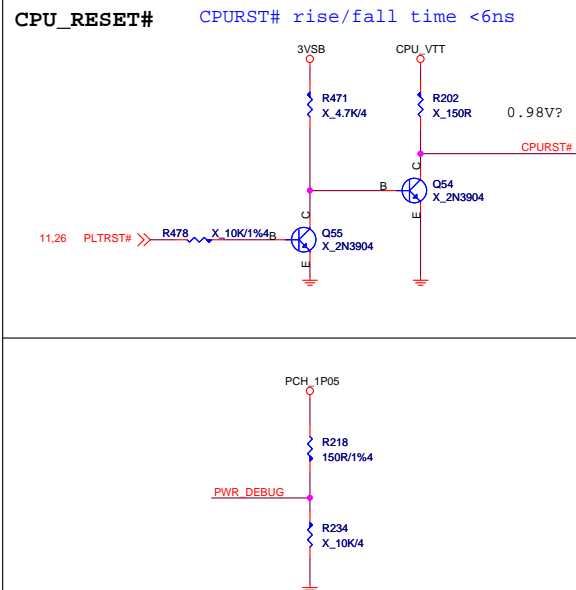


Slot Sequence:

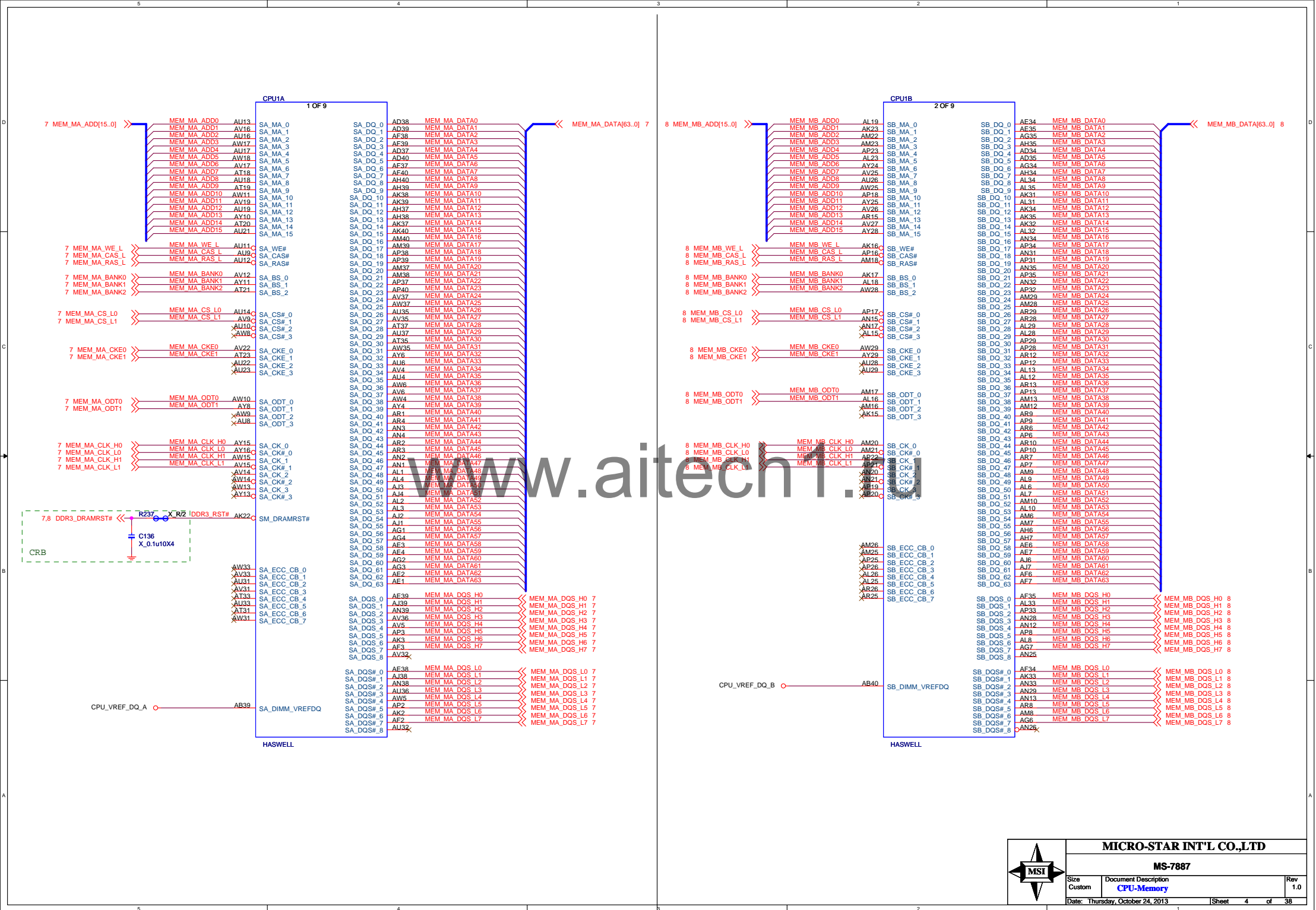
PCIE X16



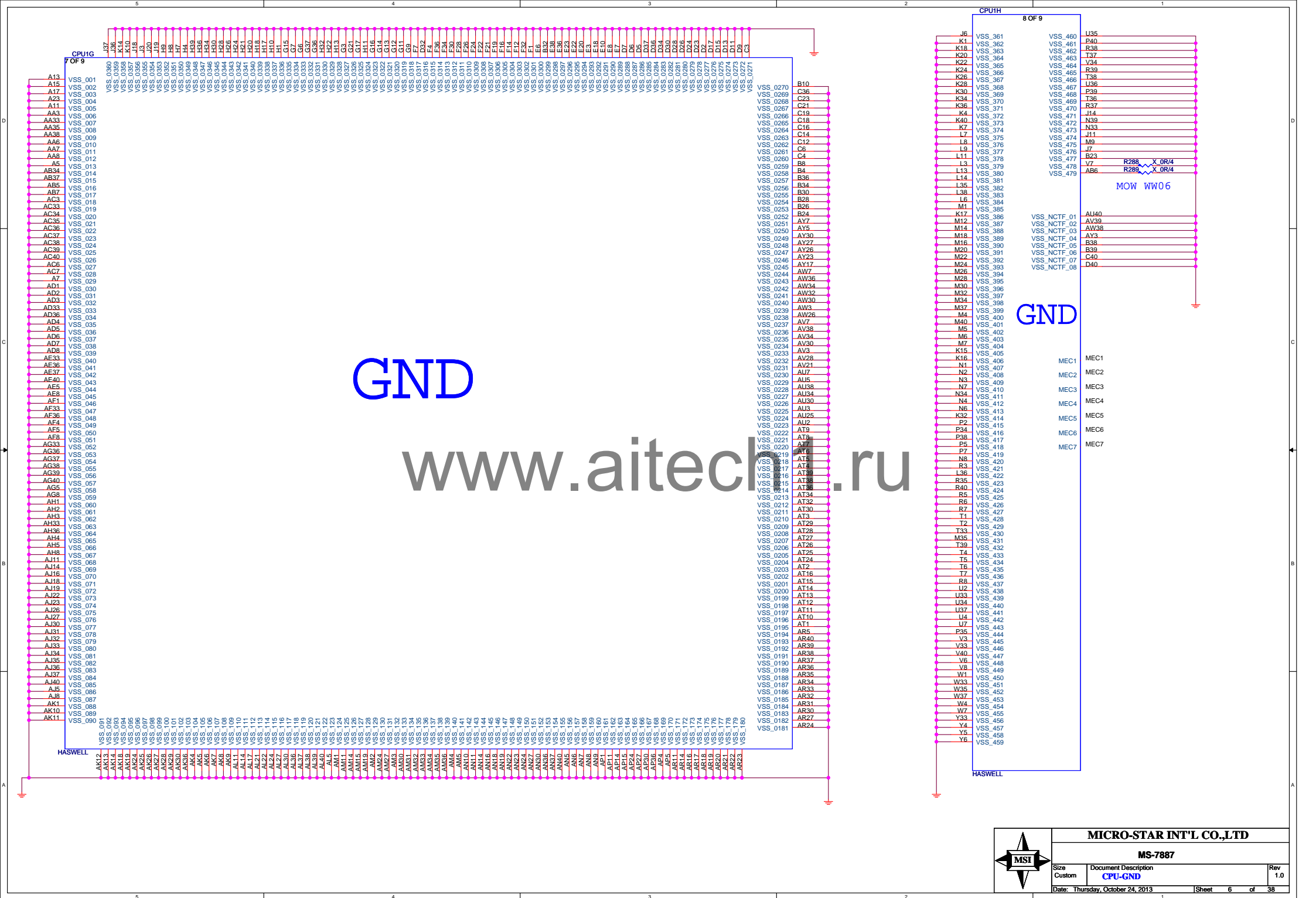
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Size Custom	Document Description <b>CPU-CNTL/CLK/MISC</b>	Rev 1.0
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GND

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GND



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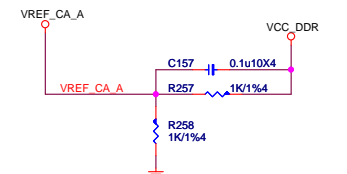
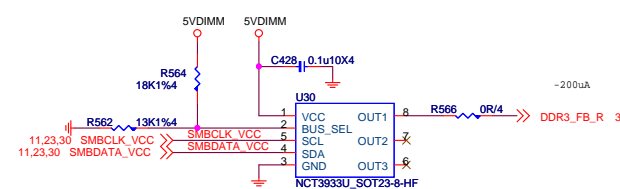
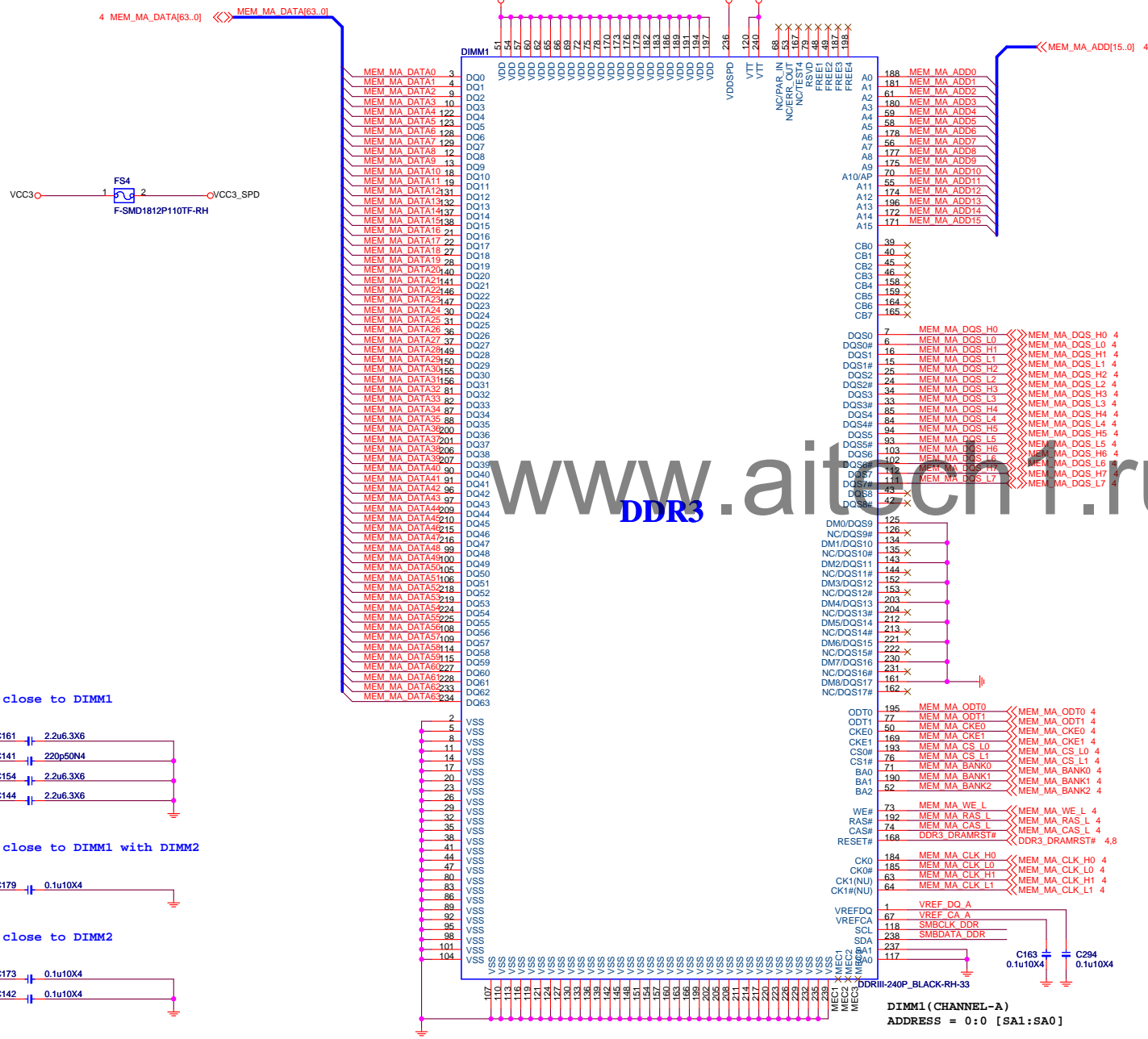
MS-7887

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Custom	CPU-GND	1.0
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# DDRIII DIMM\_A0

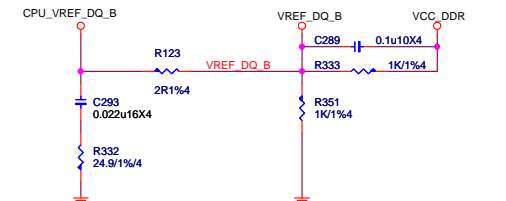
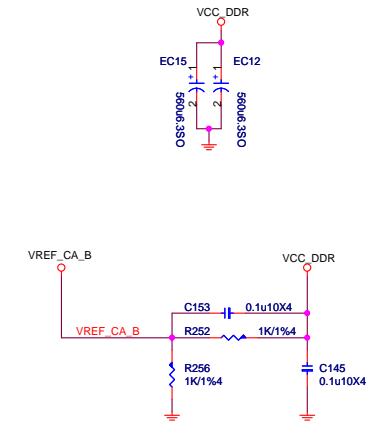
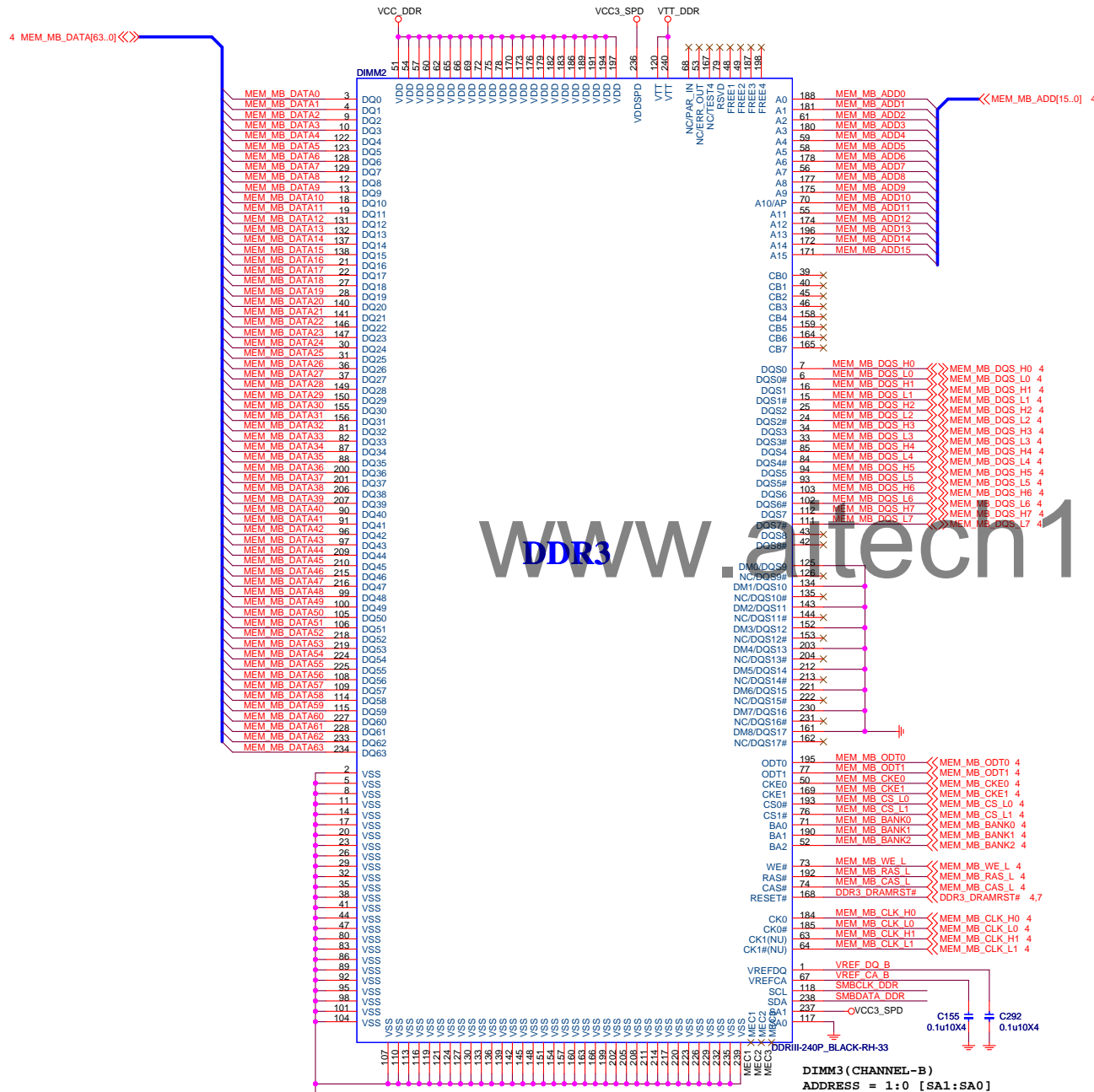
## UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



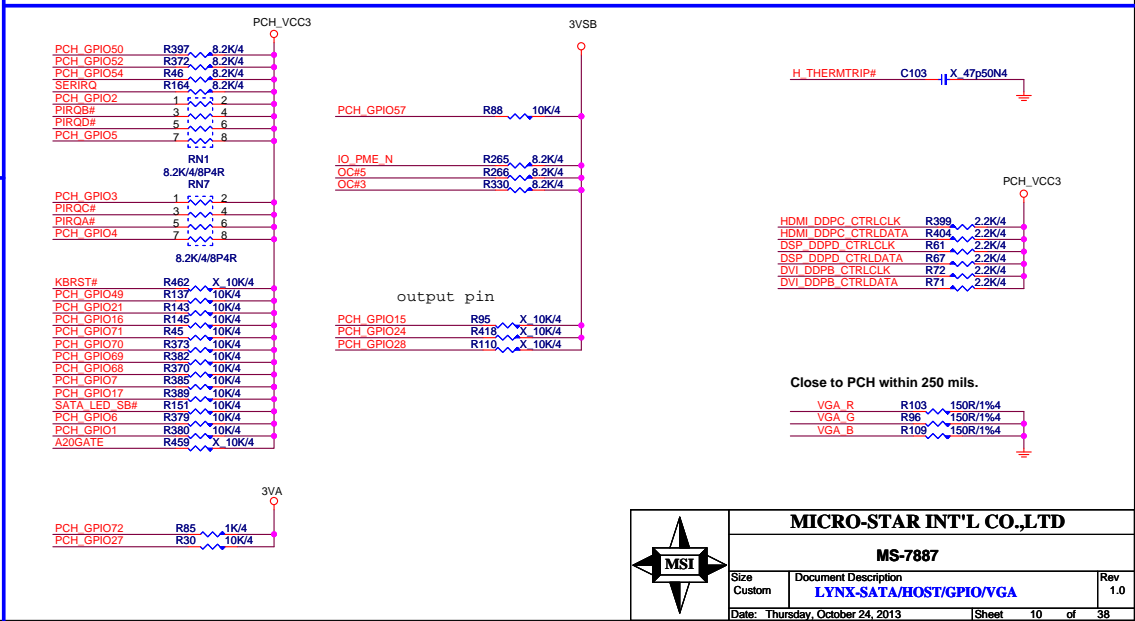
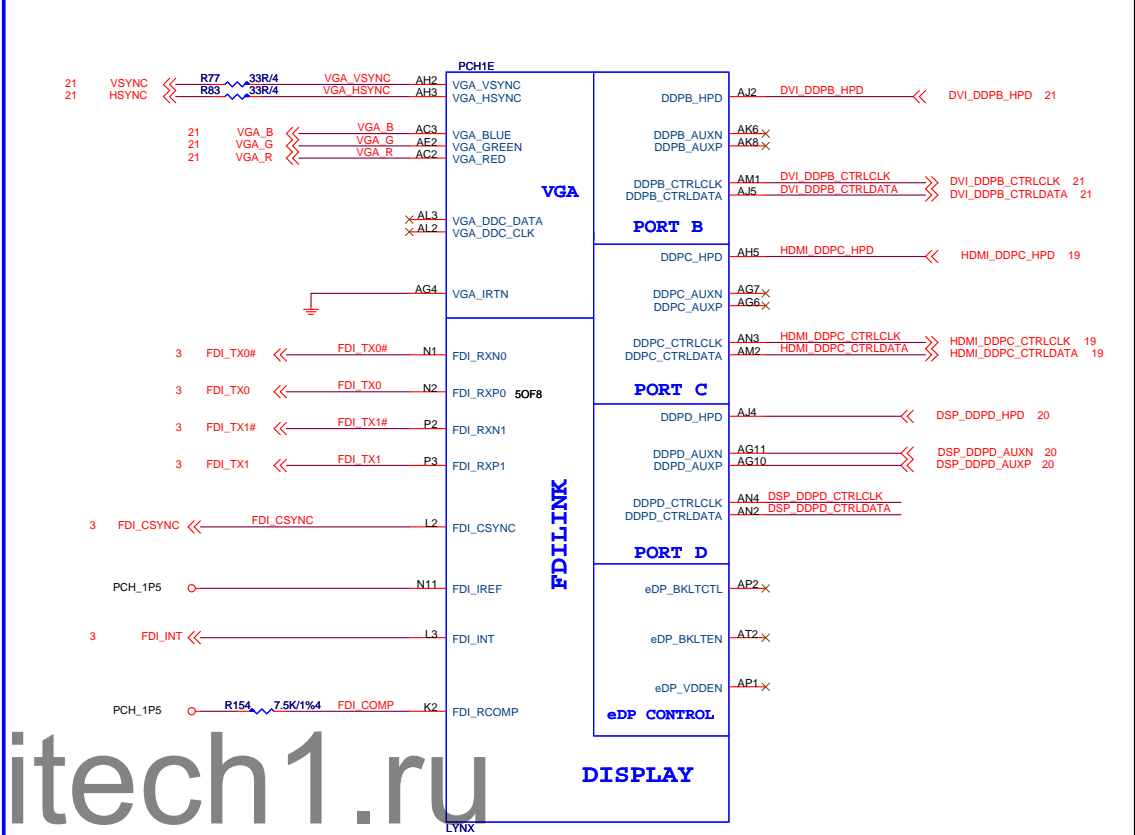
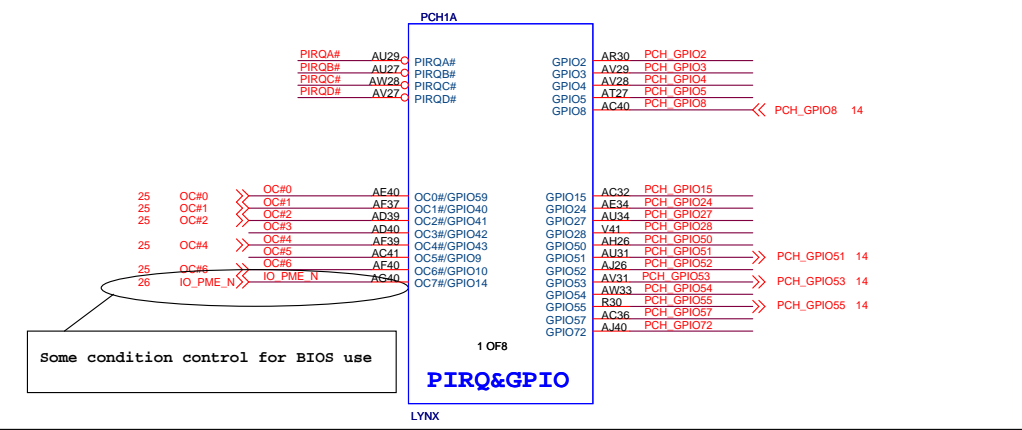
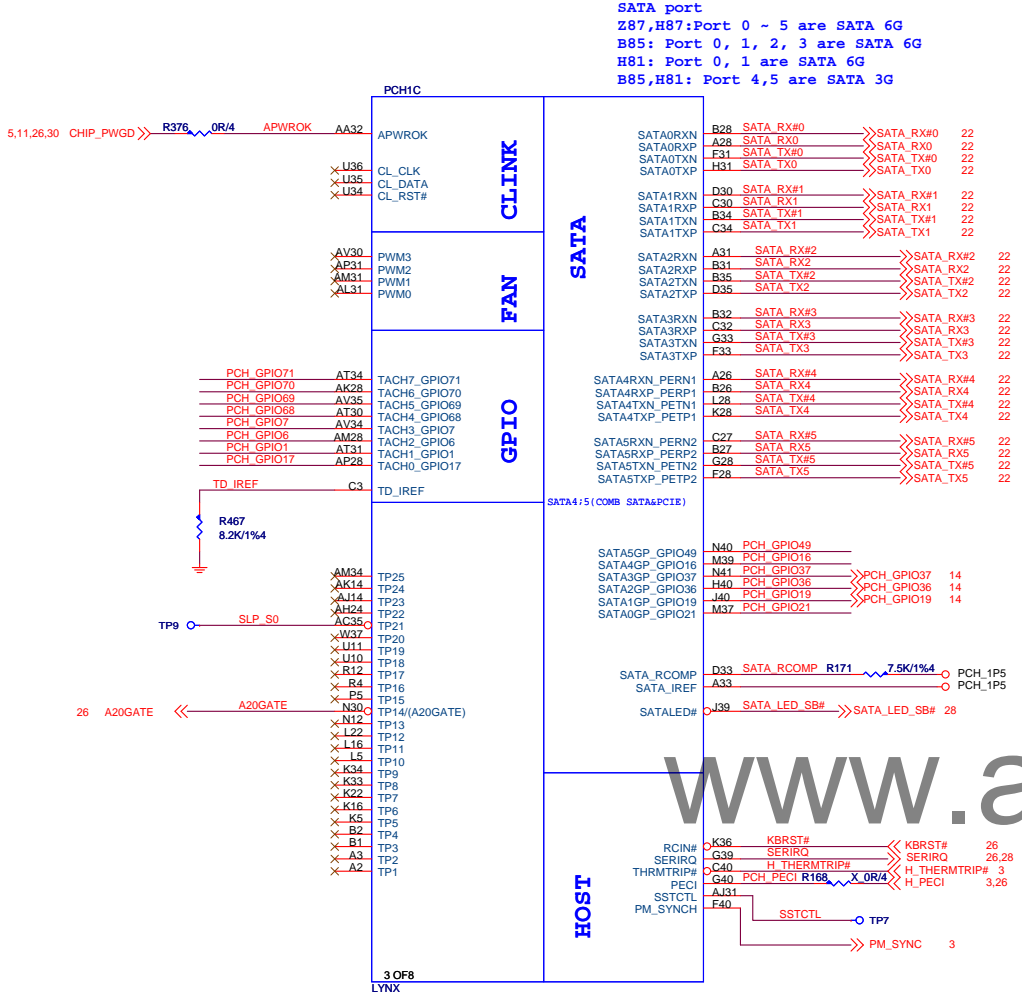
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7887</b>		
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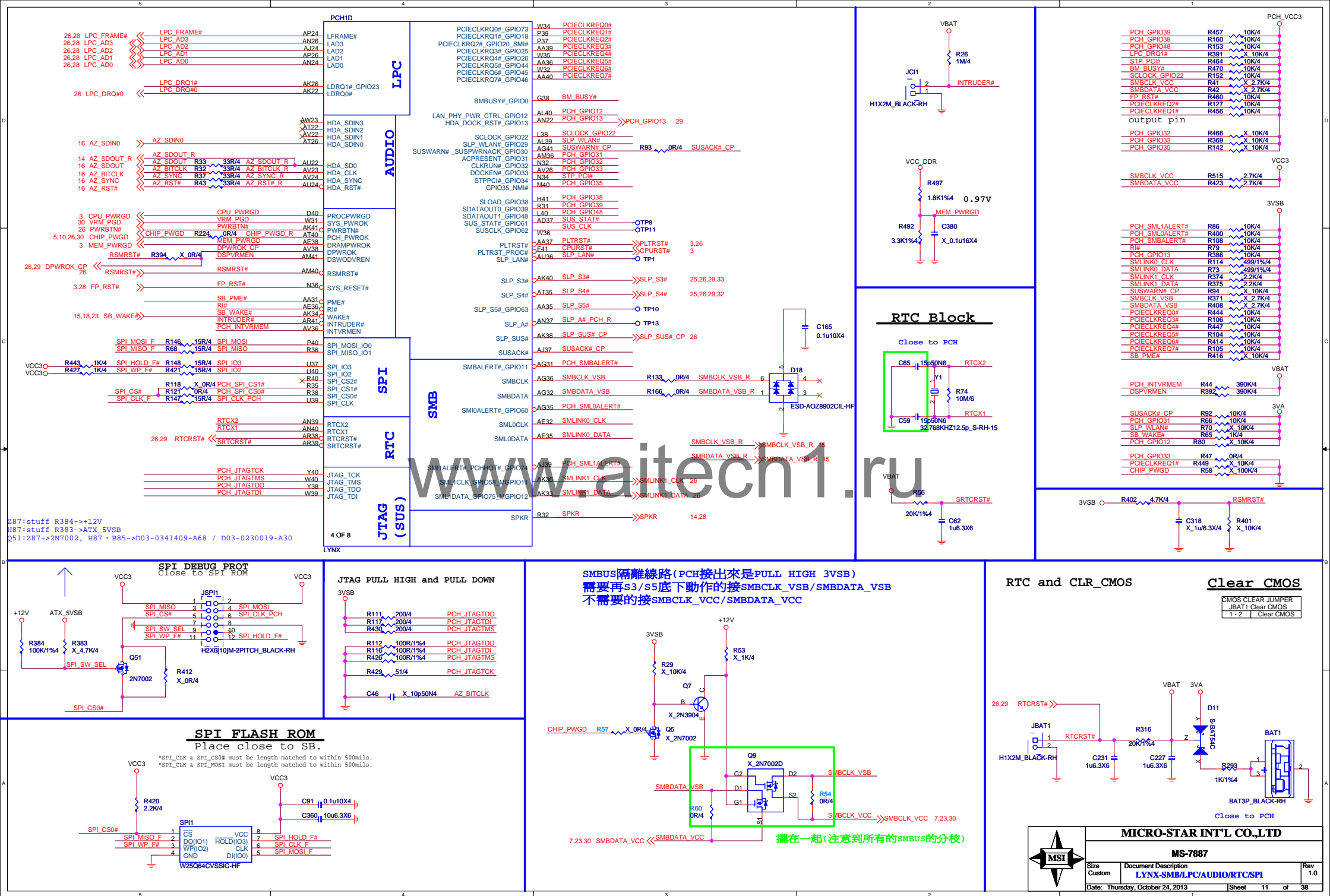
# DDR3 DIMM\_B0



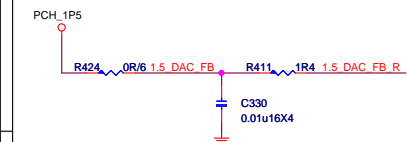
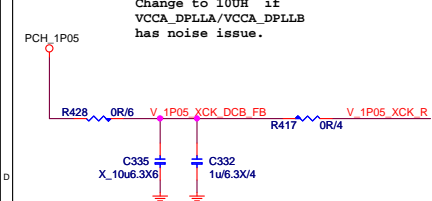
		<b>MICRO-STAR INT'L CO.,LTD</b>	
		<b>MS-7887</b>	
Size	Custom	Document Description	Rev 1.0
		<b>DDR III DIMM 2</b>	
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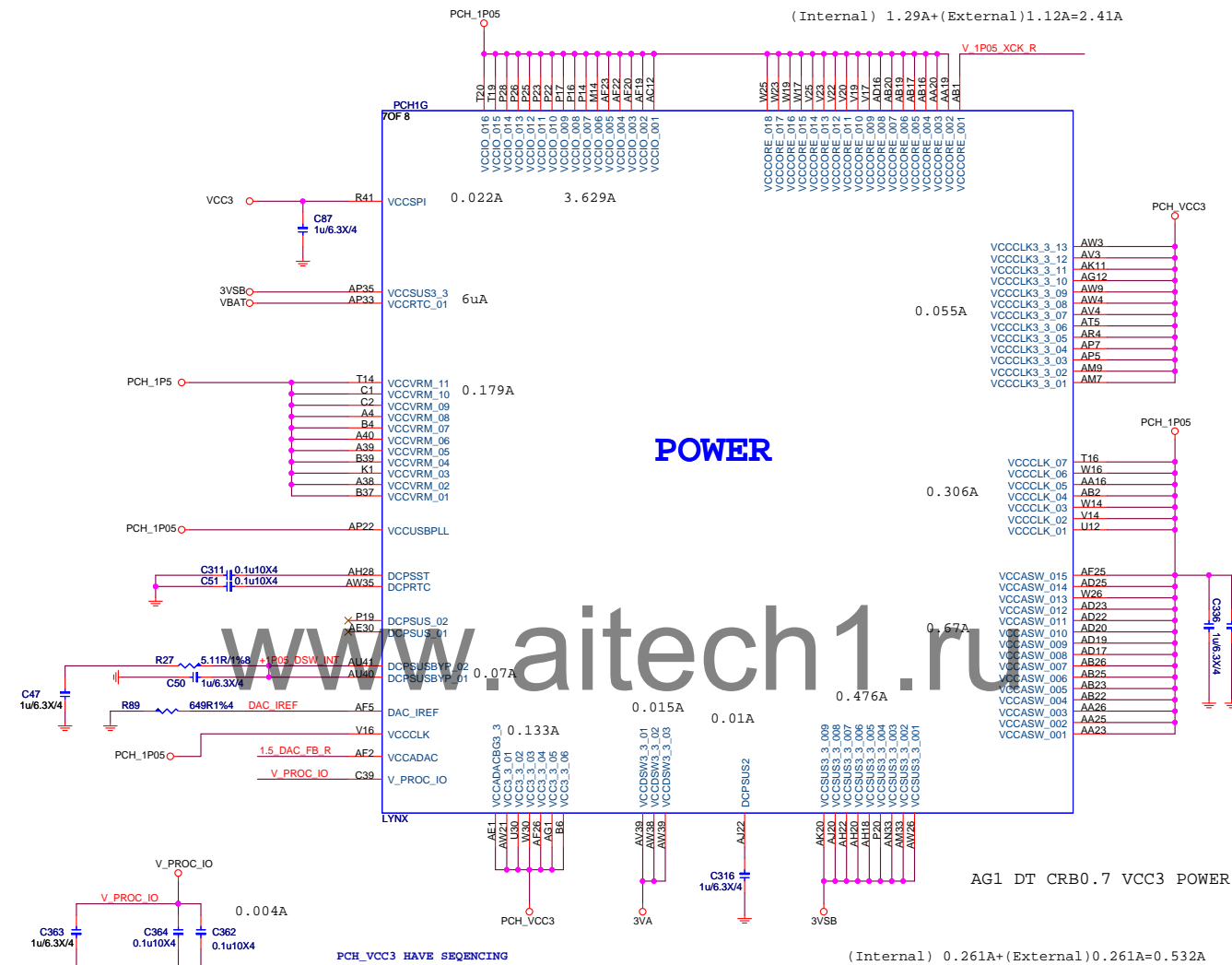




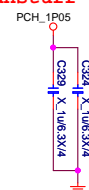
(Internal) 1.29A+(External)1.12A=2.41A



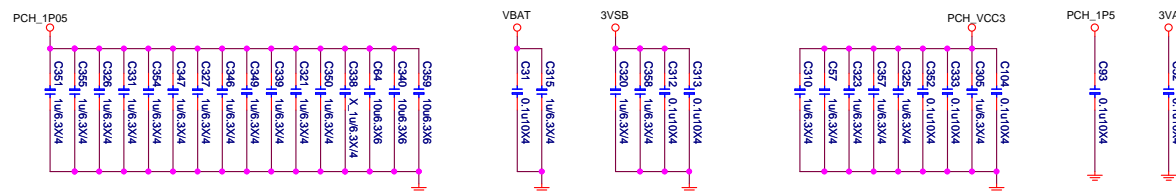
**VCC3** 0.21A  
**3VA** 0.015A  
**VBAT** 6uA  
**3VSB** 0.261A  
**VCC1\_5** 0.249A  
**PCH\_1P05** 5.747A



Backside for V14,U12,T16,V16  
**unstuff**



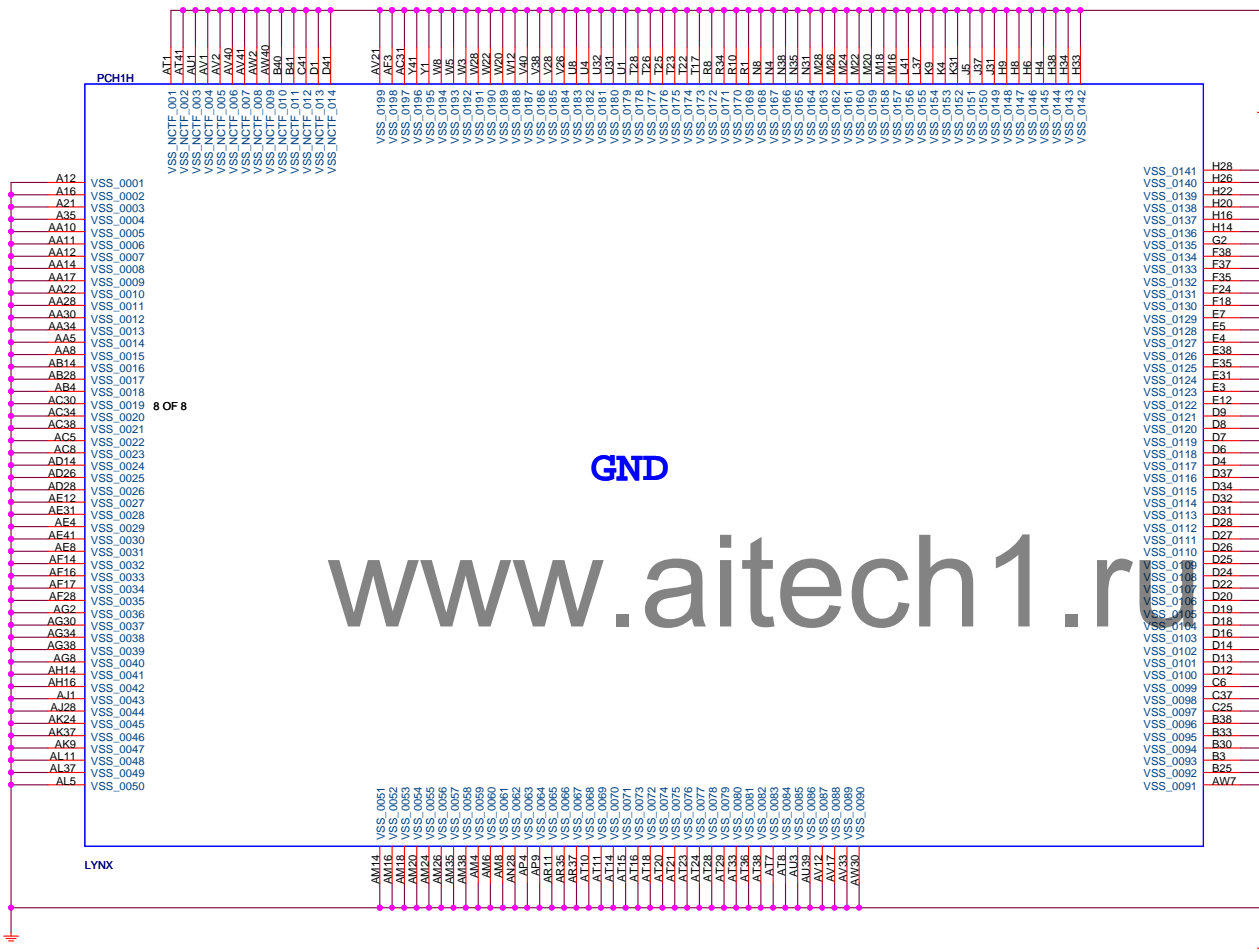
## PCH decoupling cap



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**MS-7887**

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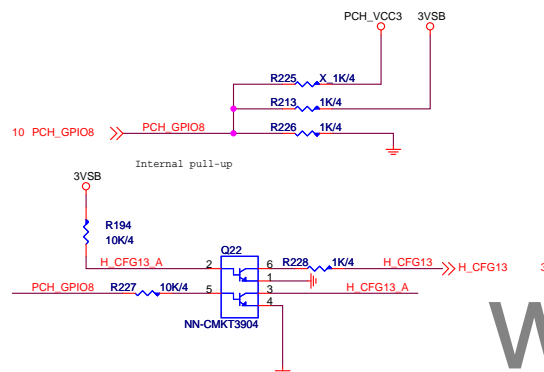
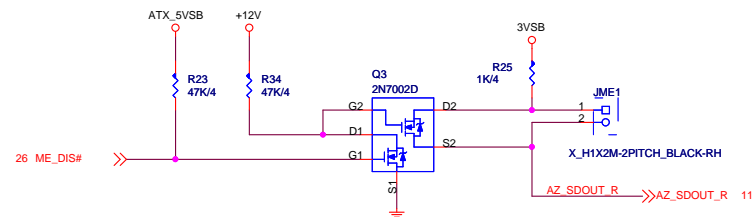


11,28 SPKR << SPKR R448 X 8.2K/4

Internal pull-DOWN

SPKR  
Default Mode:  
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:  
Connect to Vcc3\_3 with 8.2k-10k Ohm weak pullup resistor.



10 PCH\_GPIO55 >> PCH\_GPIO55 R415 X 4.7K/4

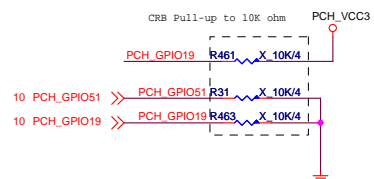
Internal pull-up

GPIO55  
Default Mode:  
Internal pull-up.

Top Block Swap Mode:  
Connect to ground with 4.7k Ohm weak pulldown resistor.

10 PCH\_GPIO53 >> PCH\_GPIO53 R36 X 1K/4

GPIO53  
Connect to ground with 1k Ohm pull-down resistor.



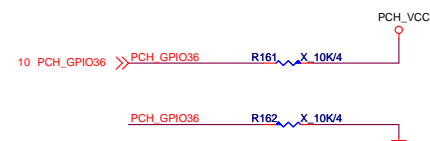
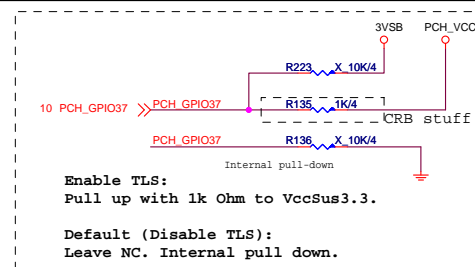
Default (SPI):  
Left both SATA1GP/GPIO19 and GPIO51 floating.  
No pull up required.

Boot from PCI:  
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.  
Leave GPIO51 Floating.

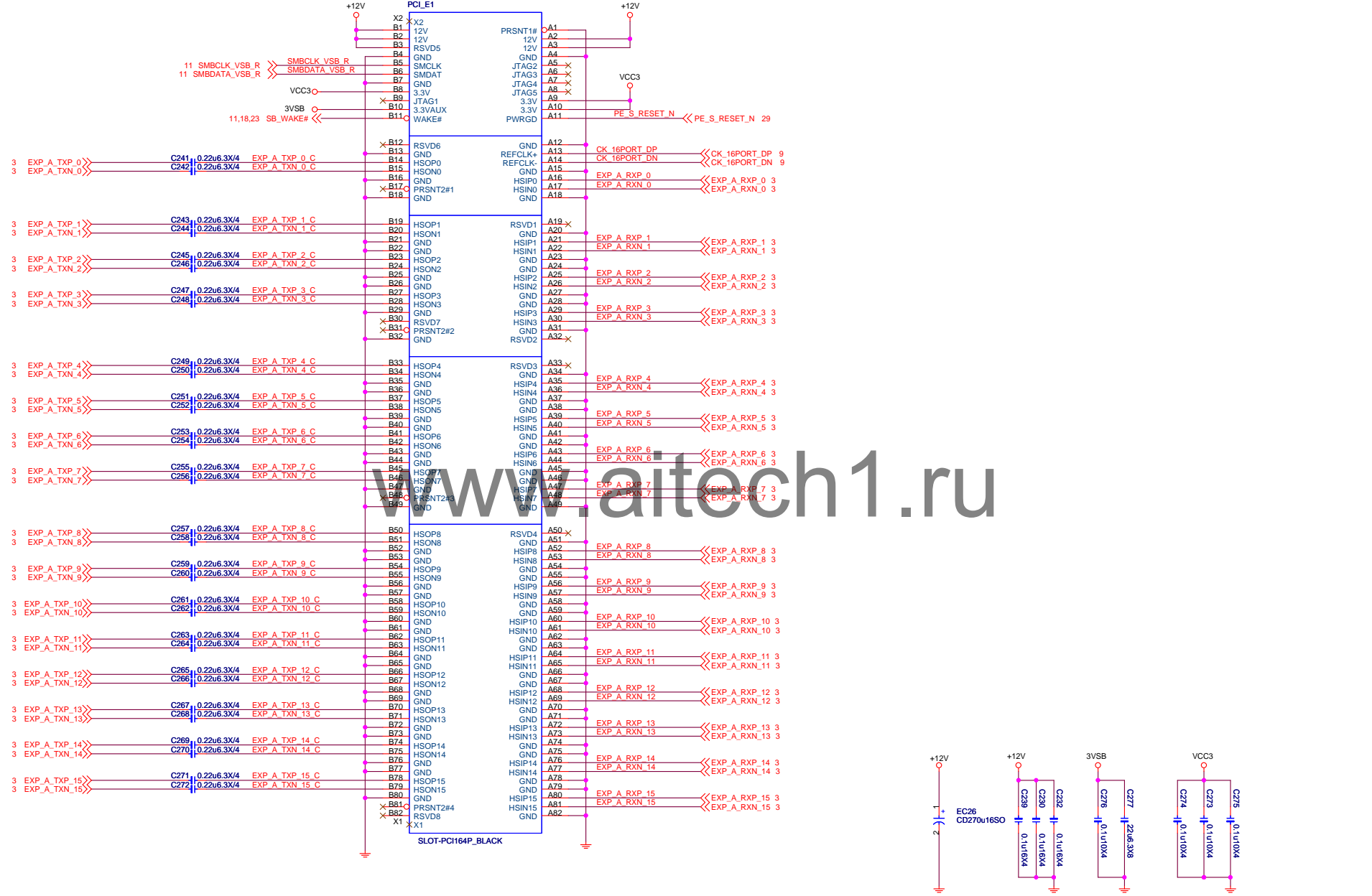
Boot from LPC:  
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default

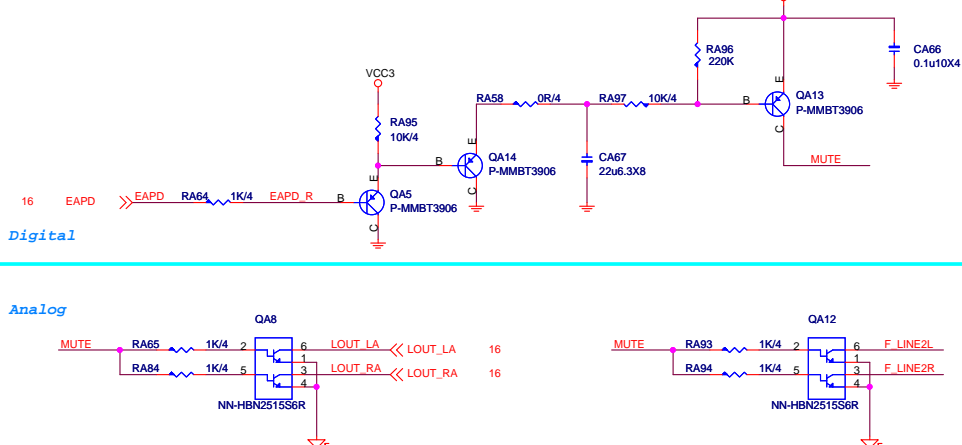
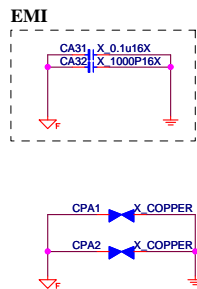
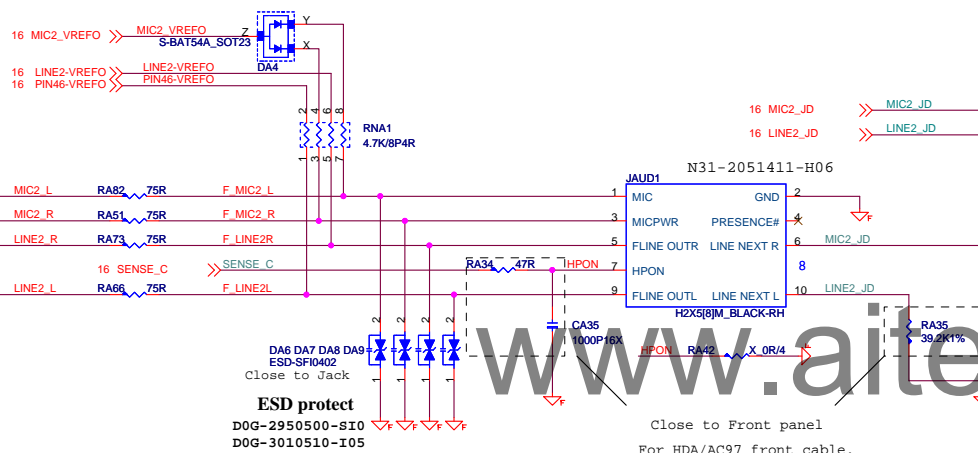


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MS-7887		
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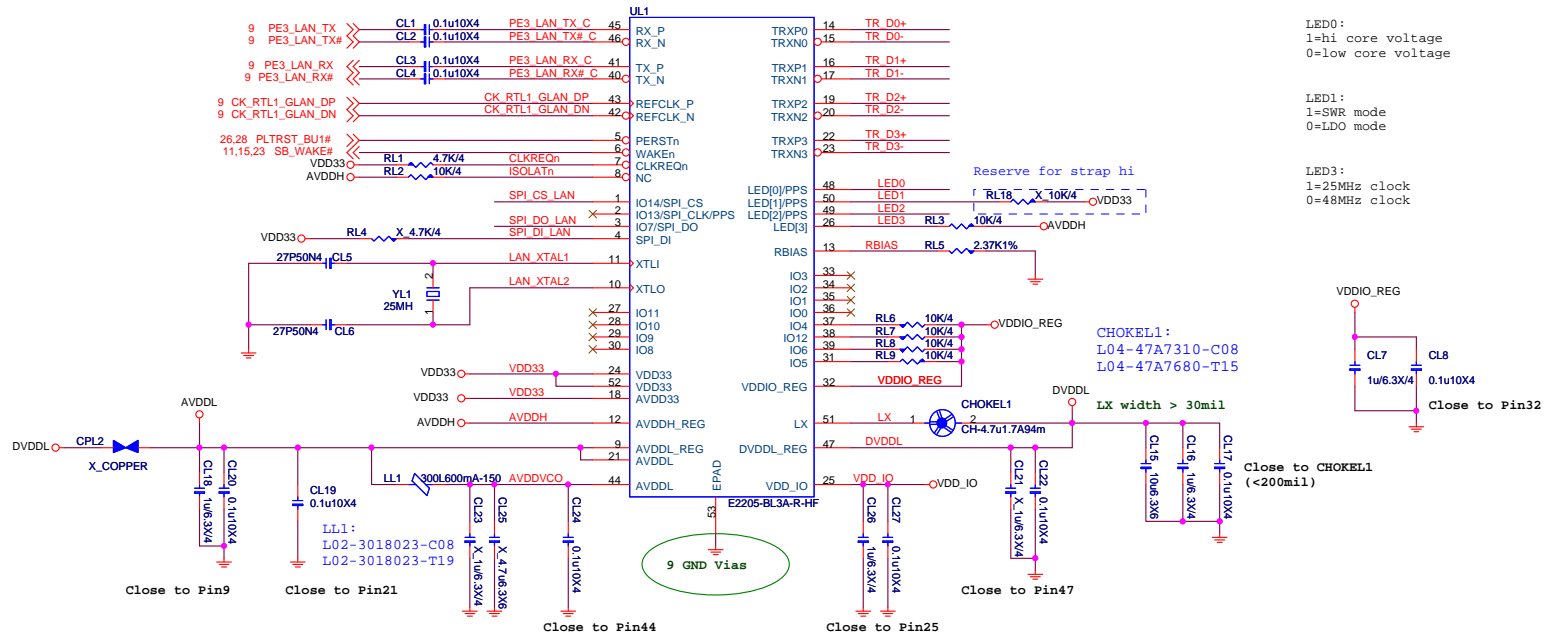


N58-42M0021-F02 (HDMI+DP+SPDIF)  
N58-06F0201-K06



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# E2205-B Giga LAN



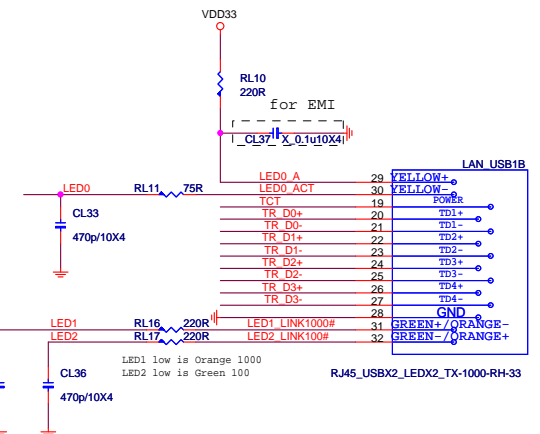
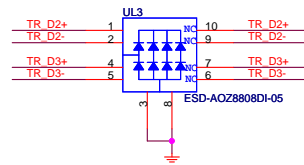
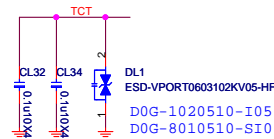
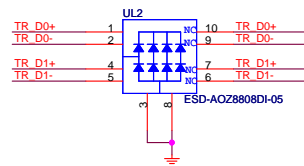
LED0:  
1=hi core voltage  
0=low core voltage

LED1:  
1=SWR mode  
0=LDO mode

LED3:  
1=25MHz clock  
0=48MHz clock

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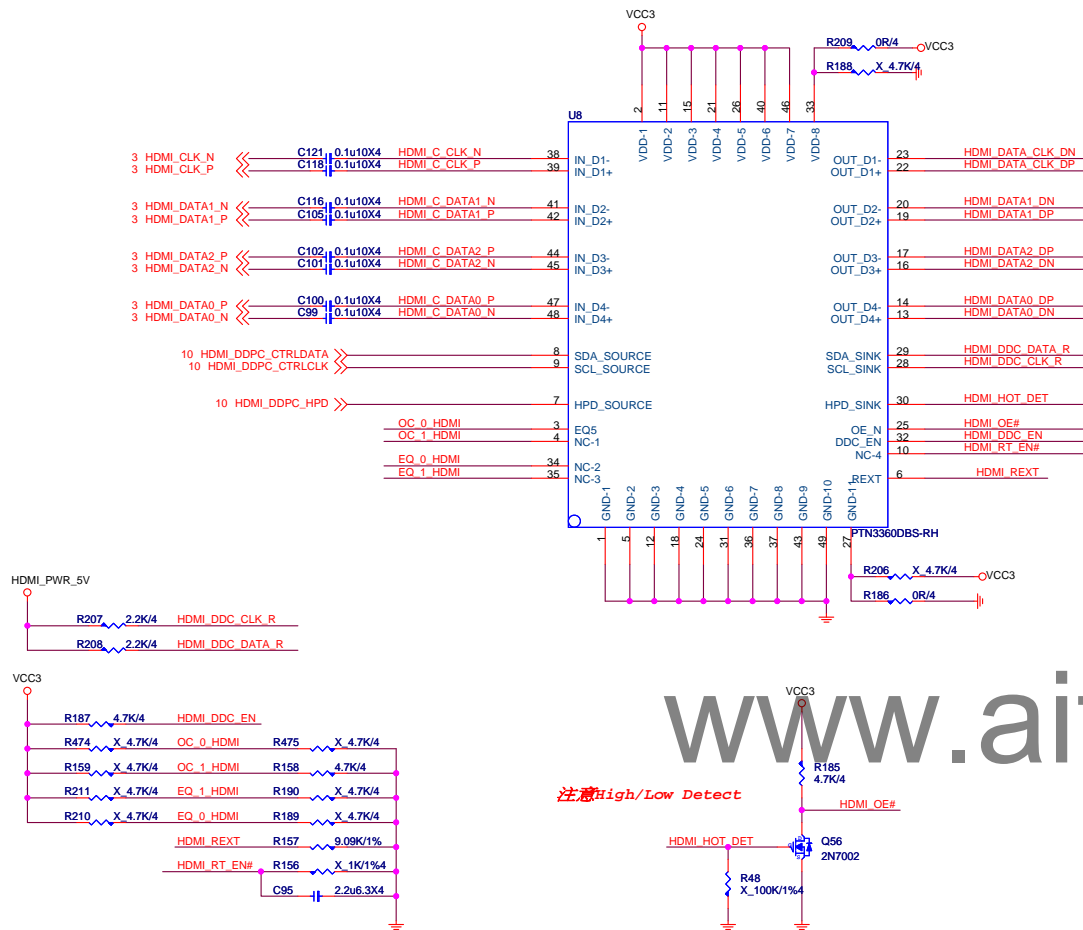
VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDDIO power trace should be wider than 30mils;  
VDDIO\_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.



- 10:  
1. Support xD, not support SPI  
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus 01:  
1. Support SPI, not support xD  
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus 11:  
1. Not support xD, not support SPI  
2. Only support PPS, PPS always at CRI013.

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# HDMI level shifter



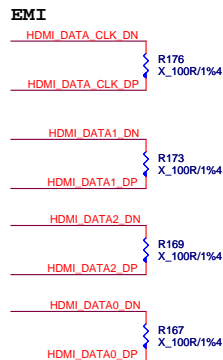
	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

注意 High/Low Detect

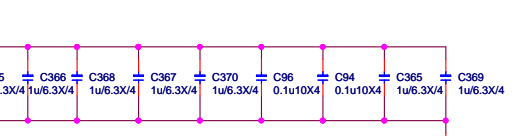
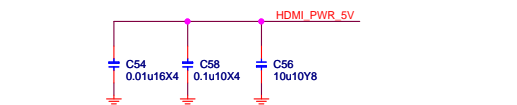
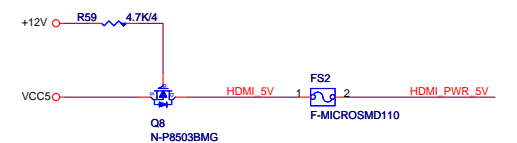
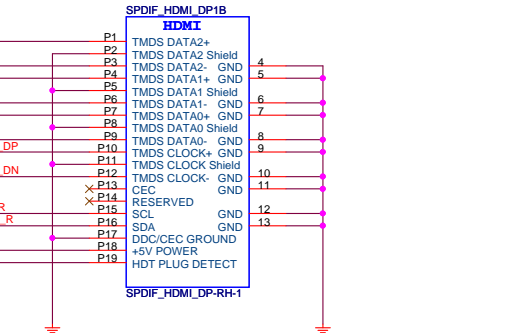
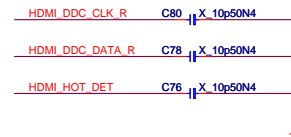
**note**  
internal pull-up at ~500K ohm.  
internal pull-down at ~500K ohm.  
internal pull-down at ~500K ohm.  
internal pull-down at ~200K ohm; 5V tolerant.  
internal pull-down at ~500K ohm.  
analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

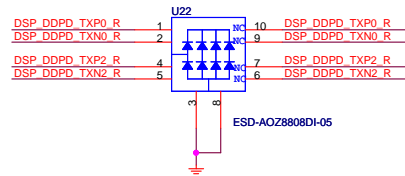
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



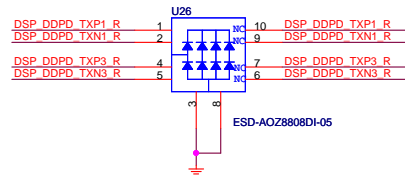
EMI cap.



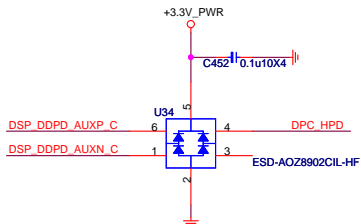
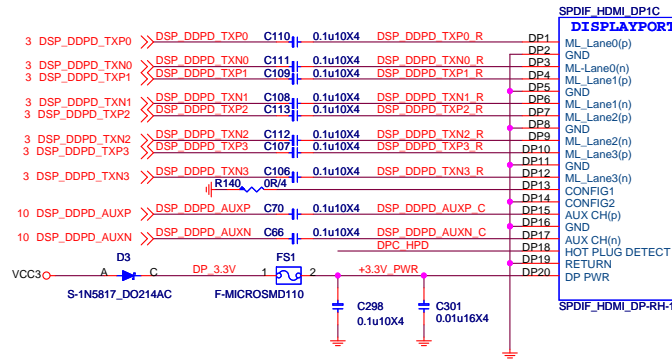
MICRO-STAR INT'L CO.,LTD			
MS-7887			
Size	Document Description	Rev	
Custom	HDMI Connector	1.0	
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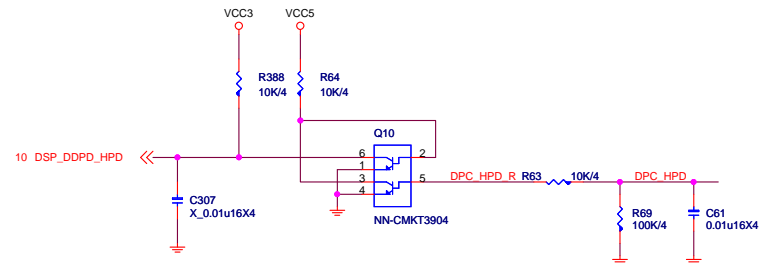
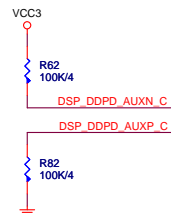
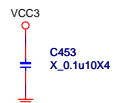
AVL:D0G-06A050C-A68



DP



D0G-0200529-A68 Main  
D0G-0100619-I05 AVL

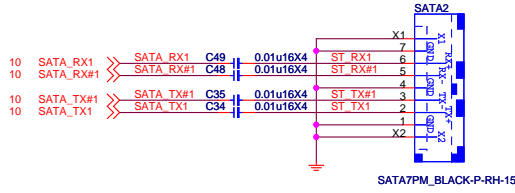
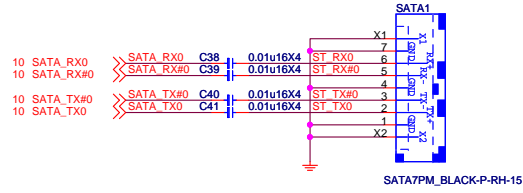




SATA port  
 Z87,H87:Port 0 ~ 5 are SATA 6G  
 B85: Port 0, 1, 2, 3 are SATA 6G  
 H81: Port 0, 1 are SATA 6G  
 B85,H81: Port 4,5 are SATA 3G

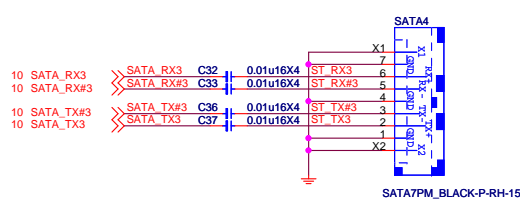
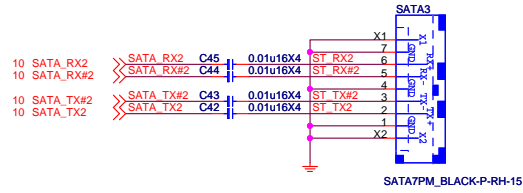
### SATA 6G PORT 0,1

3.0 BLACK

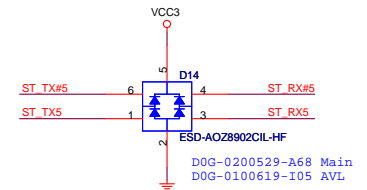
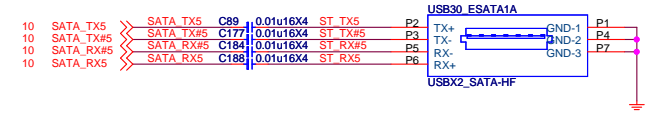


### SATA 6G PORT 2,3

3.0 BLACK

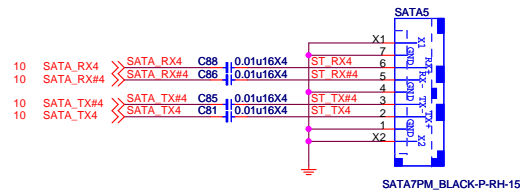


### eSATA 6G PORT 4



### SATA 6G PORT 4

3.0 BLACK



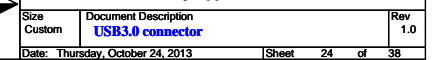
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	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7887</b>		
	Size Custom	Document Description <b>MINI PCIE + BT + WIFI</b>	Rev 1.0
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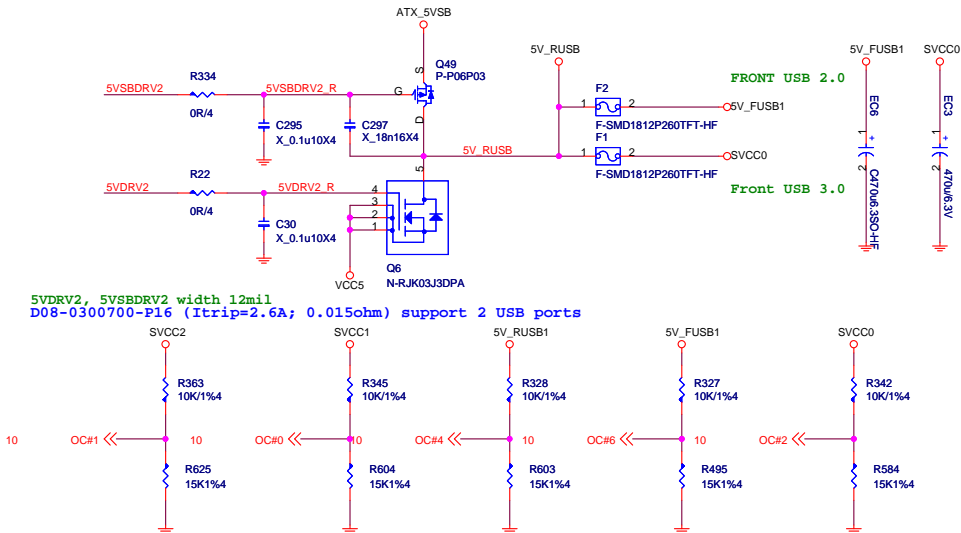
Pin connection diagram for the 2X10 connector. The diagram shows two rows of pins. The top row (pins 1-10) is connected to MB\_USB\_5D+, MB\_USB\_5D-, SSTX5P, SSTX5N, SSRX5P, SSRX5N, SVCC0, and GND. The bottom row (pins 1-10) is connected to MB\_USB\_4D+, MB\_USB\_4D-, SSTX4P, SSTX4N, SSRX4P, SSRX4N, SVCC0, and GND. The connector is labeled JUSB2 and 2X10\_CONNECTOR. The board is labeled BH2X10[20]\_2PITCH\_BLACK-RH-1.

Figure 10 shows the pin connections for the USB30 ESATA1B and USBX2 SATA\_HF connectors. The diagram is divided into two main sections: USB30 ESATA1B (top) and USBX2 SATA\_HF (bottom). The USB30 ESATA1B section shows pins B1-B9, A1-A3, A5-A6, and A8-A9. The USBX2 SATA\_HF section shows pins B1-B4, X5-X8, A1-A4, X1-X4, and A8-A9. The diagram also shows the internal connections between the two connectors, including the USB30 ESATA1B and USBX2 SATA\_HF labels.

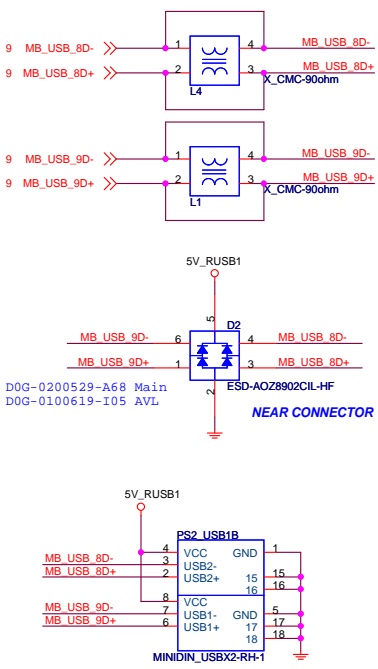
Pin	Signal	Connector
9	MB_USB_3D+	USB30 ESATA1B B1
9	MB_USB_3D+	USB30 ESATA1B B3
9	SSRX2N	USB30 ESATA1B B5
9	SSRX2P	USB30 ESATA1B B6
9	SSTX2N	USB30 ESATA1B B8
9	SSTX2P	USB30 ESATA1B B9
9	MB_USB_2D+	USB30 ESATA1B A1
9	MB_USB_2D+	USB30 ESATA1B A3
9	SSRX3N	USB30 ESATA1B A5
9	SSRX3P	USB30 ESATA1B A6
9	SSTX3N	USB30 ESATA1B A8
9	SSTX3P	USB30 ESATA1B A9
	VBUS-2	USBX2 SATA_HF B1
	GND-D-2	USBX2 SATA_HF B4
	GND-5	USBX2 SATA_HF X5
	X6	USBX2 SATA_HF X6
	X7	USBX2 SATA_HF X7
	X8	USBX2 SATA_HF X8
	VBUS-1	USBX2 SATA_HF A1
	GND-D-4	USBX2 SATA_HF A4
	X1	USBX2 SATA_HF X1
	X2	USBX2 SATA_HF X2
	X3	USBX2 SATA_HF X3
	X4	USBX2 SATA_HF X4



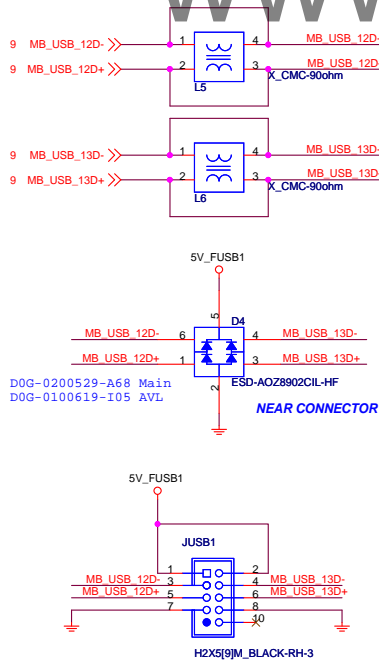
Front USB Power



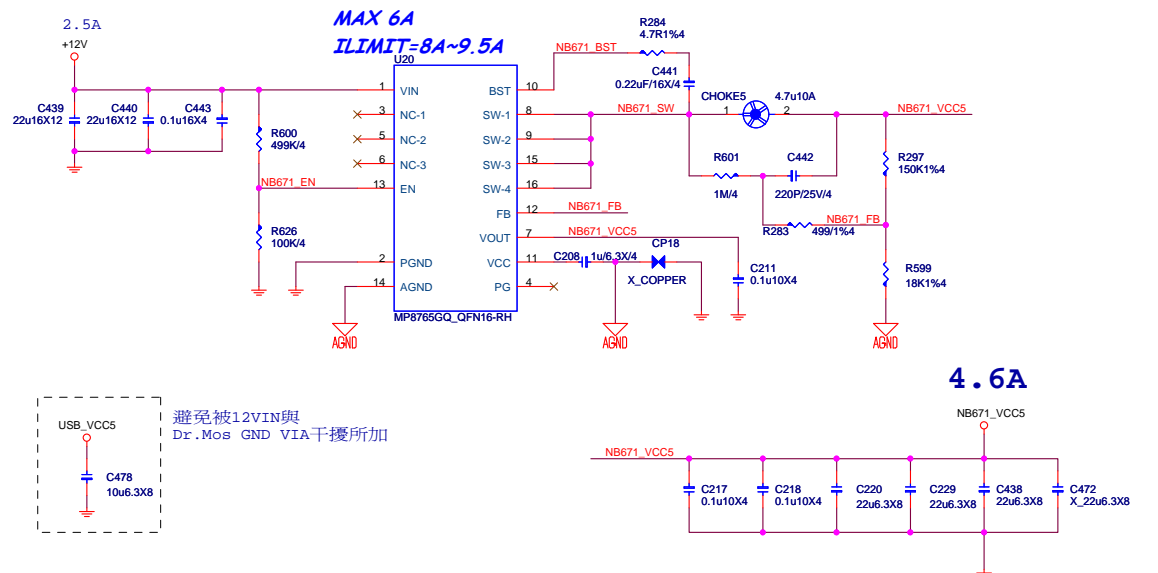
REAR USB PORT 08,09 (With PS2)



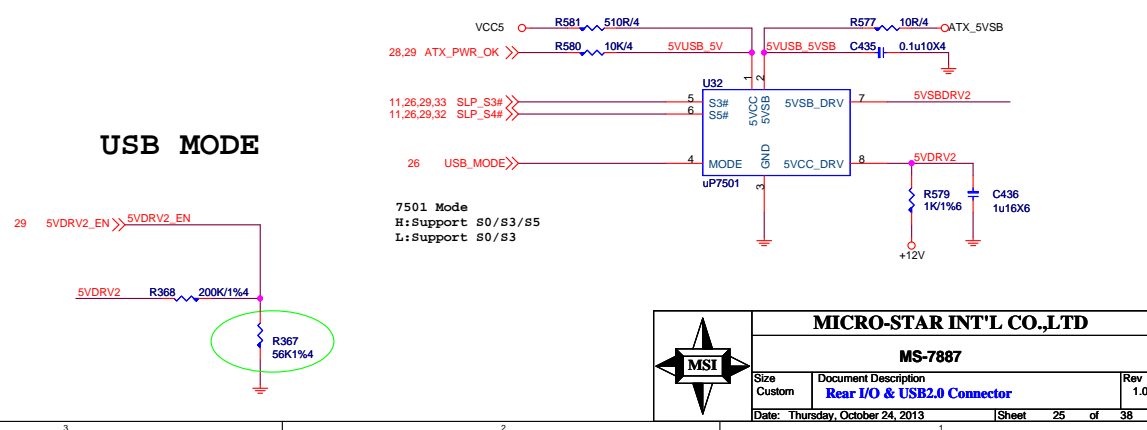
FRONT USB PORT 12,13

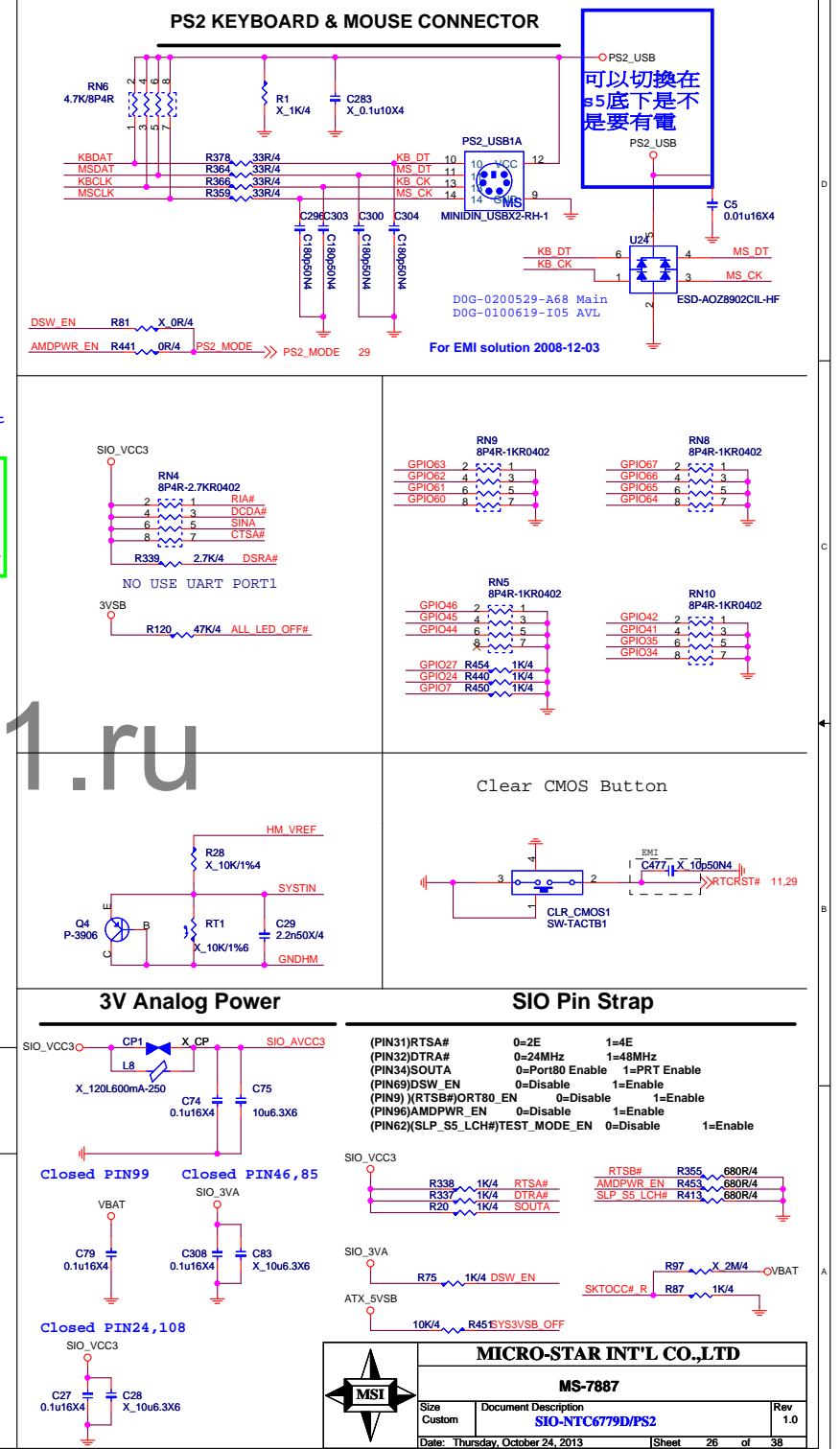
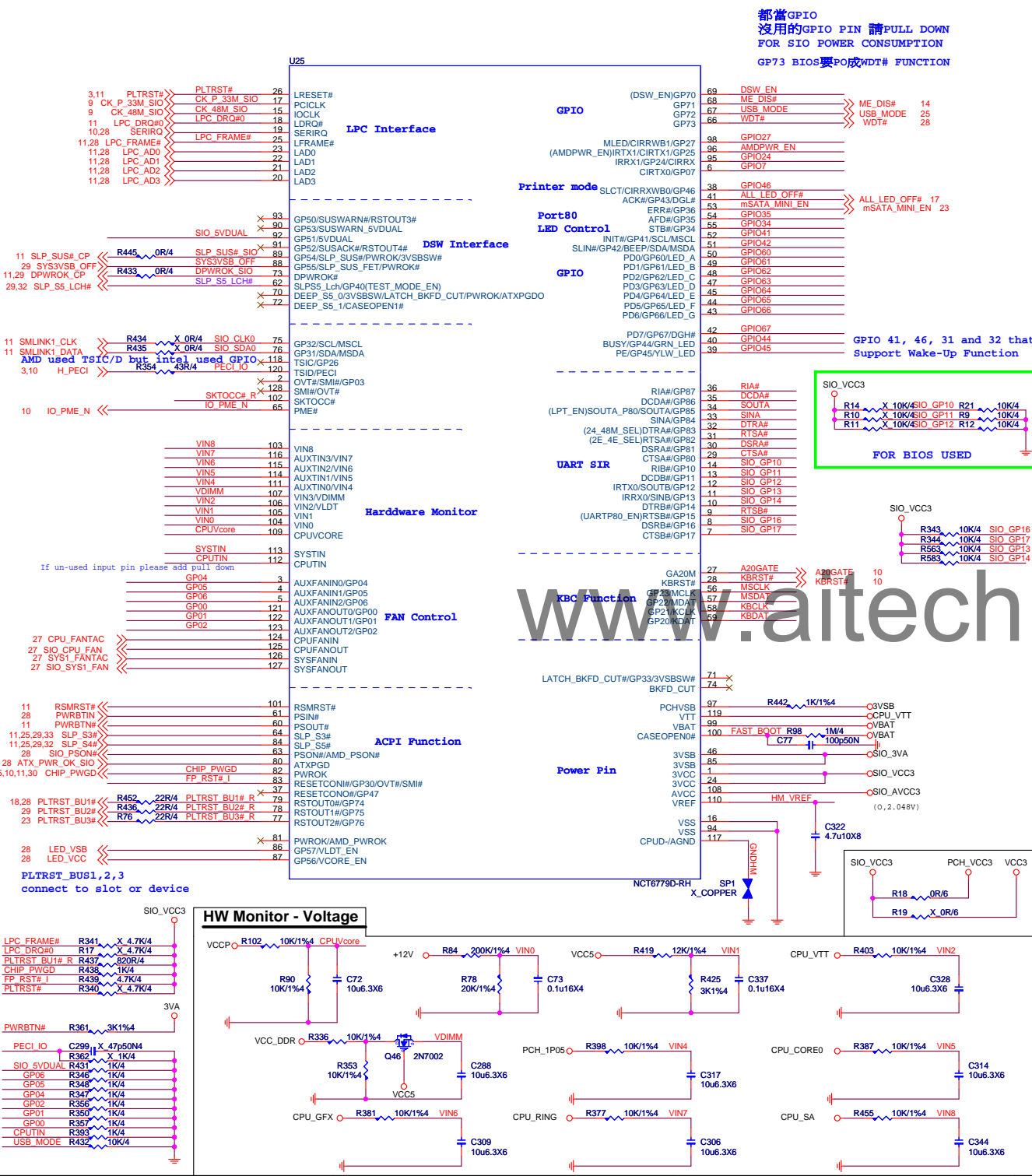


Real USB Power



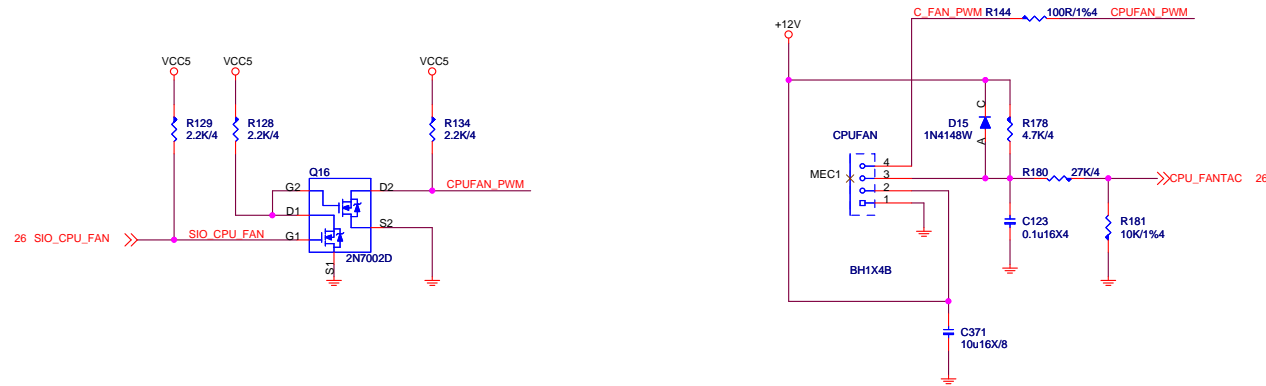
USB Power Select



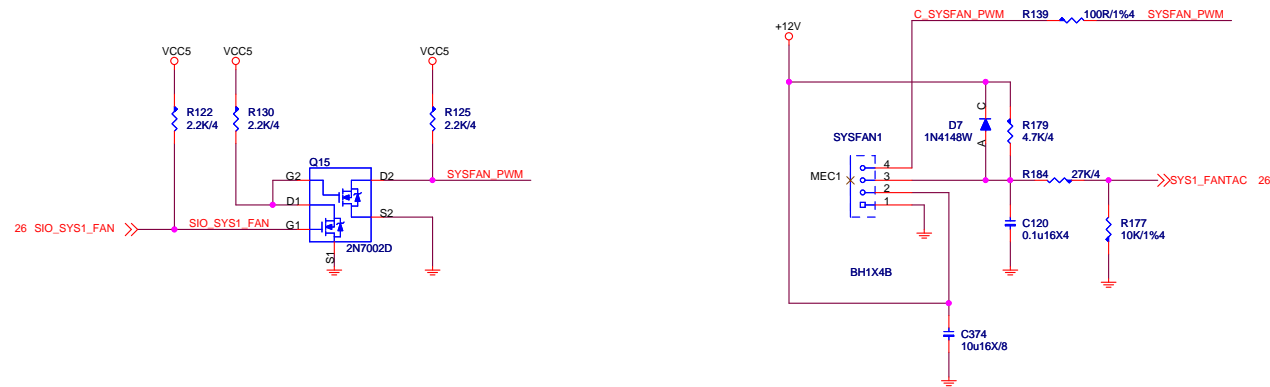


# FAN-COUNTROL CIRCUIT

CPUFAN TYPE E



SYSTEM FAN1 (PWM MODE)



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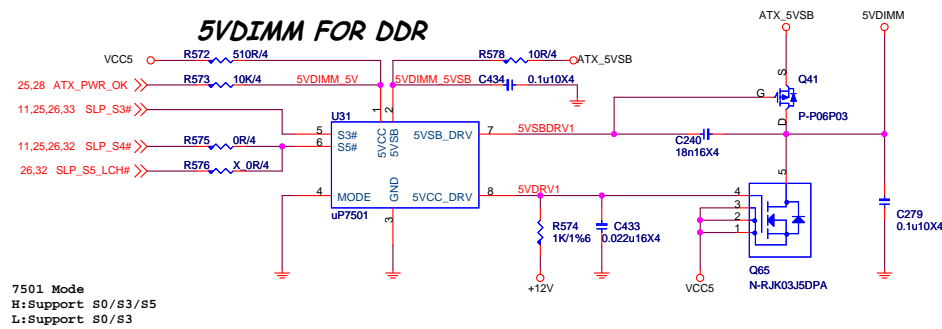
MICRO-STAR INT'L CO.,LTD

MS-7887

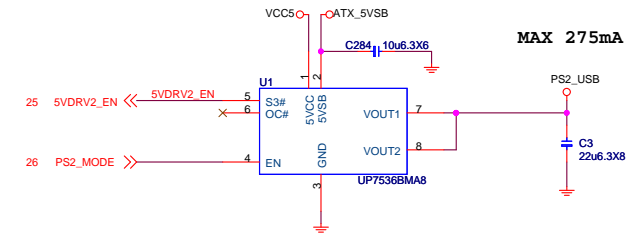
Size Custom	Document Description FAN Control	Rev 1.0
Date: Thursday, October 24, 2013	Sheet 27 of 38	



## 5VDIMM FOR DDR

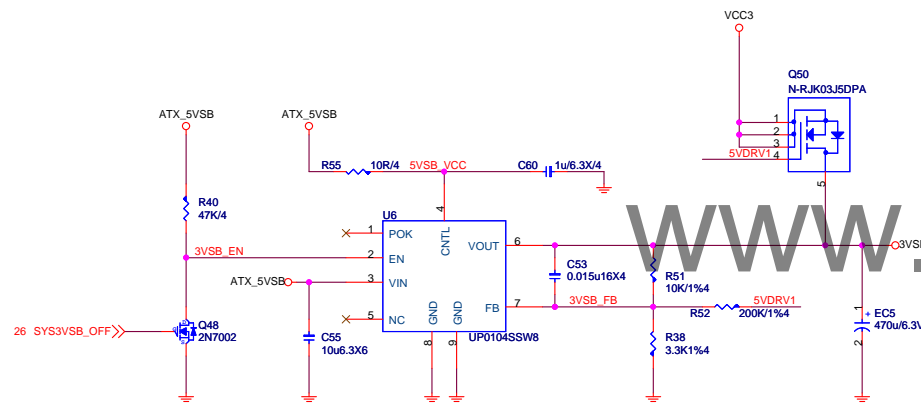


## PS2 Power

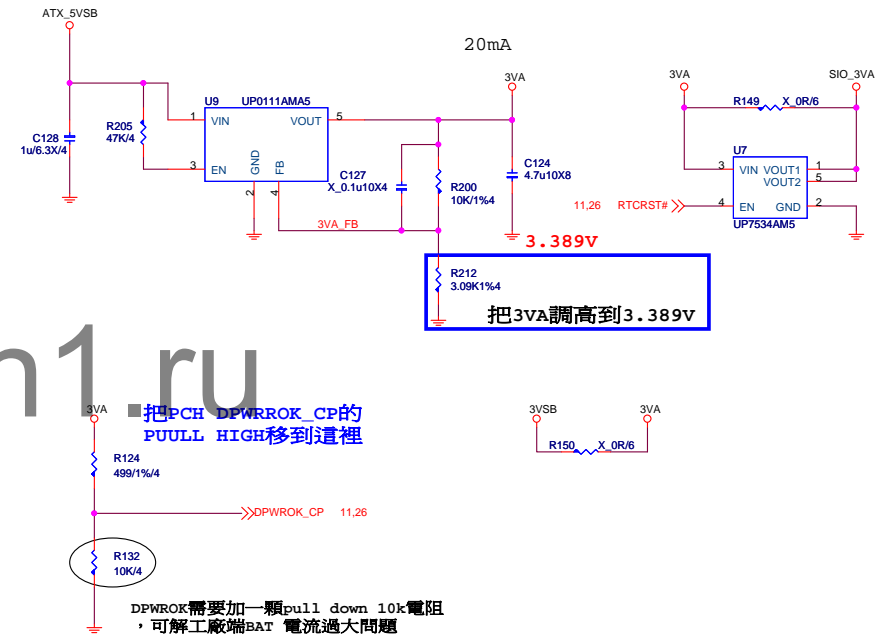


## 3VSB

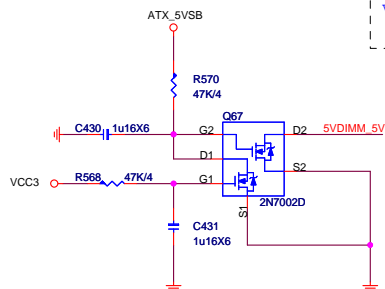
3.041A



## 3VA

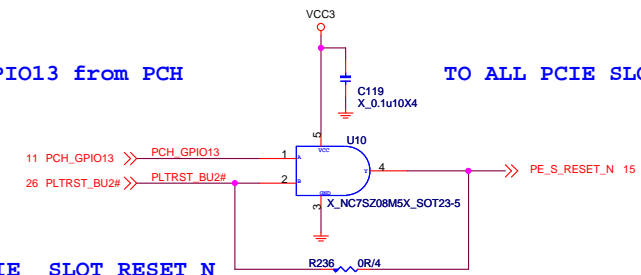


```
| For power 700W solution (only for uP7501+uP7506 for 3VSB solution)|
| The power supply VCC3 delay 12ms after VCC5 assert.|
| The chip U7501 5VDRV1 work when the VCC5 ready|
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but|
| VCC3 not ready and let the 3VSB sequence fail.
```



GPI013 from PCH

TO ALL PCIE SLOT RESET#



```
PCIE _SLOT_RESET_N
from SIO RESET_BUS2
```

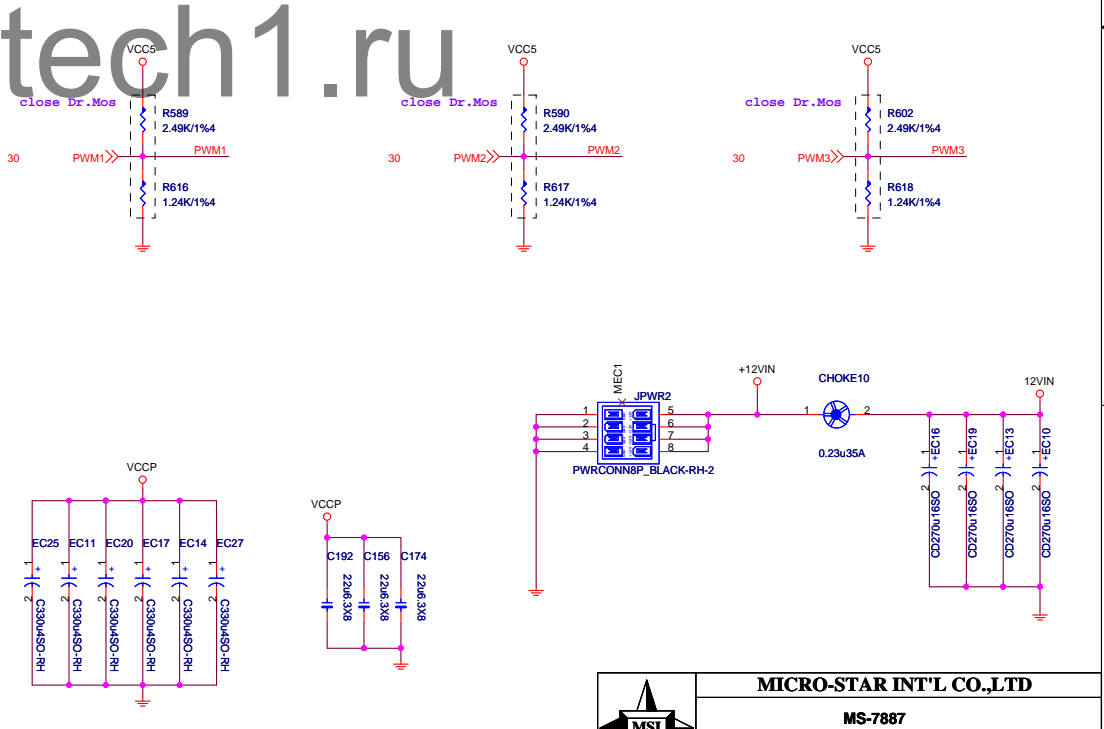
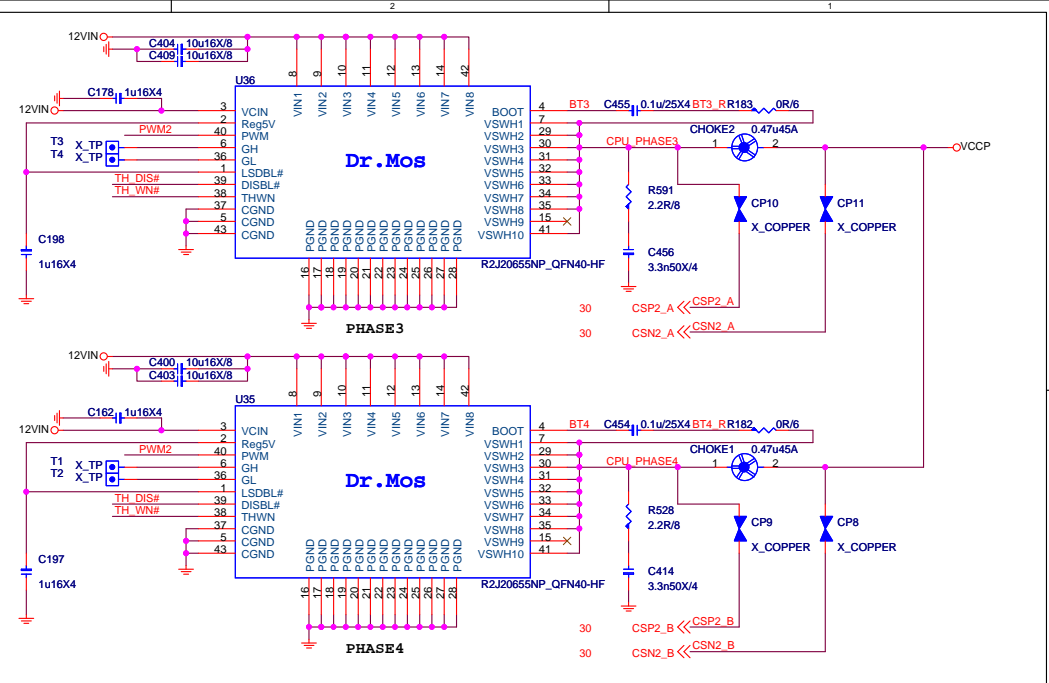


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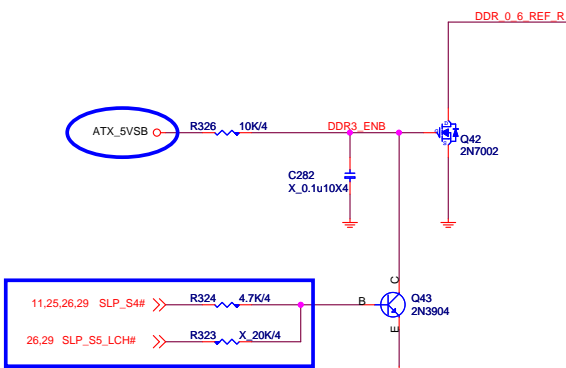
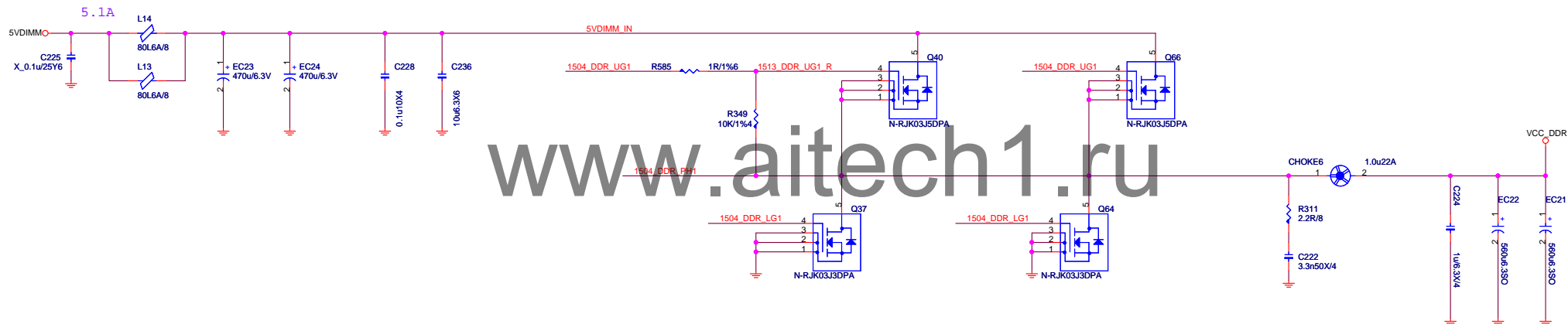
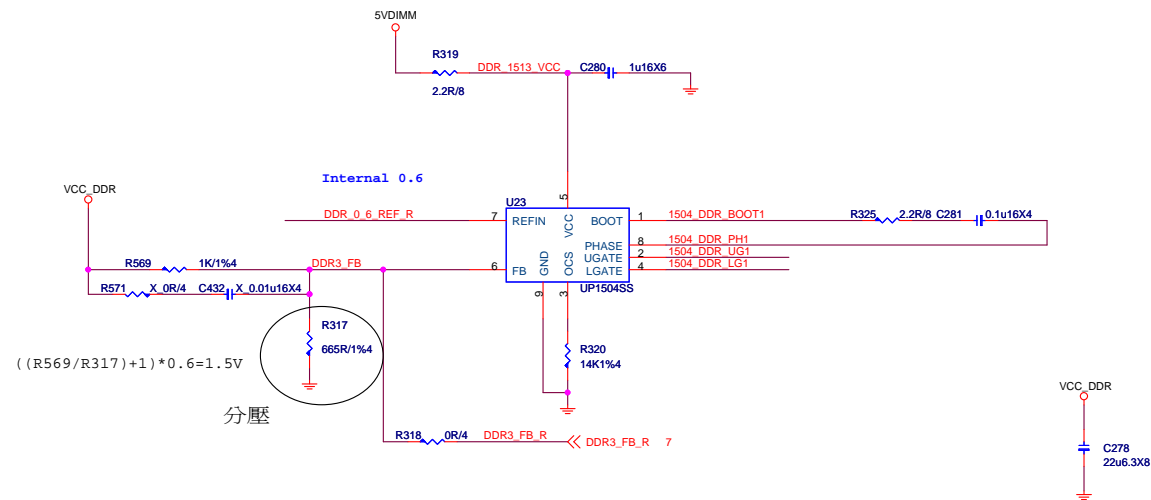
Size Custom	Document Description <b>ACPI controller UPI</b>	Rev 1.0
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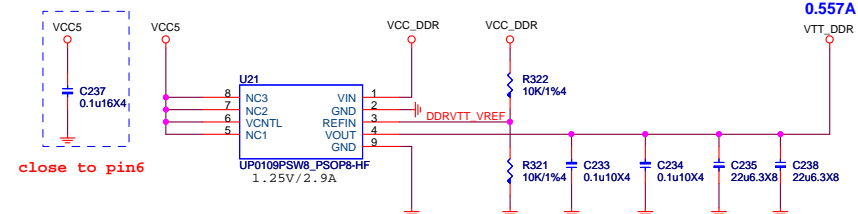


**PCH Core 6A**

**$R_{320}=14K\ ohm$**



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



P.S. Only for meet Intel power down sequence.



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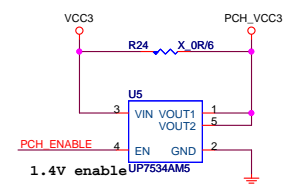
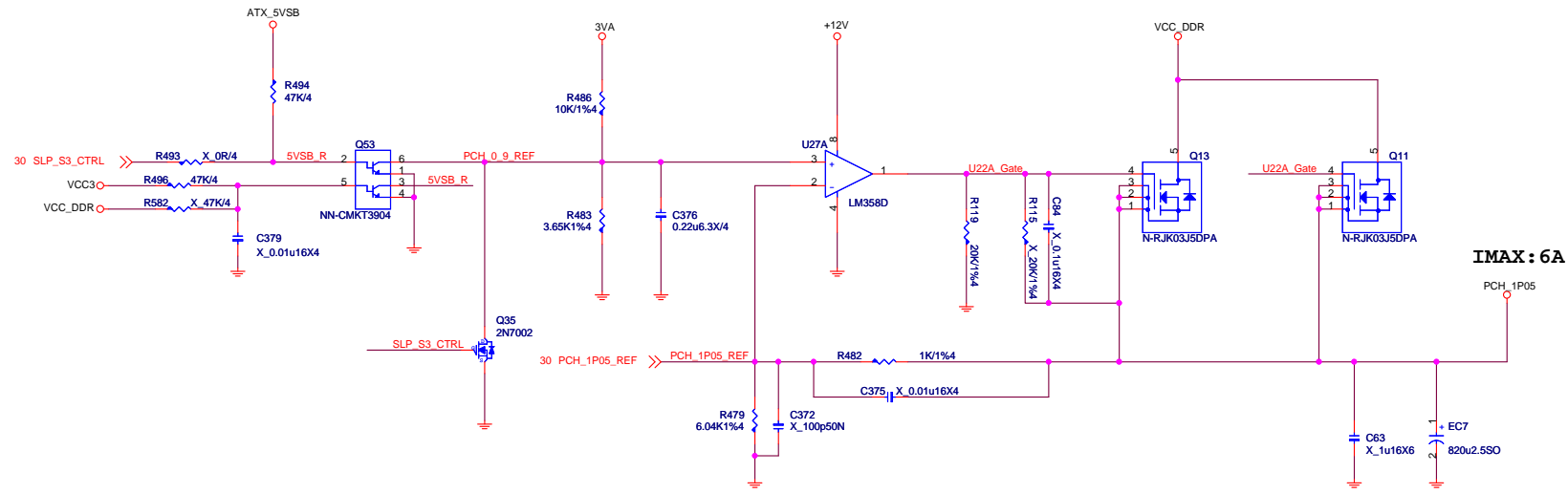
Size Custom	Document Description <b>DDR POWER - UP1504S -2PHASE</b>	Rev 1.0
Date: Thursday, October 24, 2013		Sheet 32 of 38

PCH Power:1.05V  
PCH Core 6A

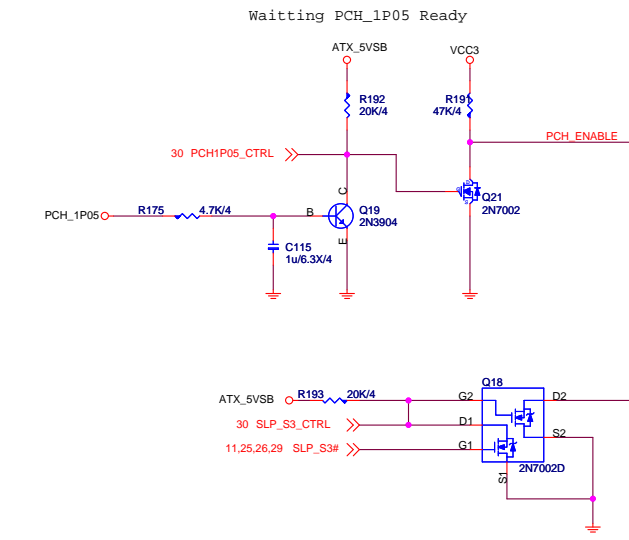
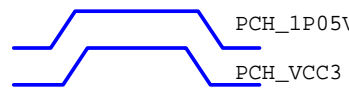
Iripple=1.80A  
5\*1=5A>1.80A  
Iout ripple = 5A

PCH Power:3.3V

0.133A



VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



PCH Power:1.5V

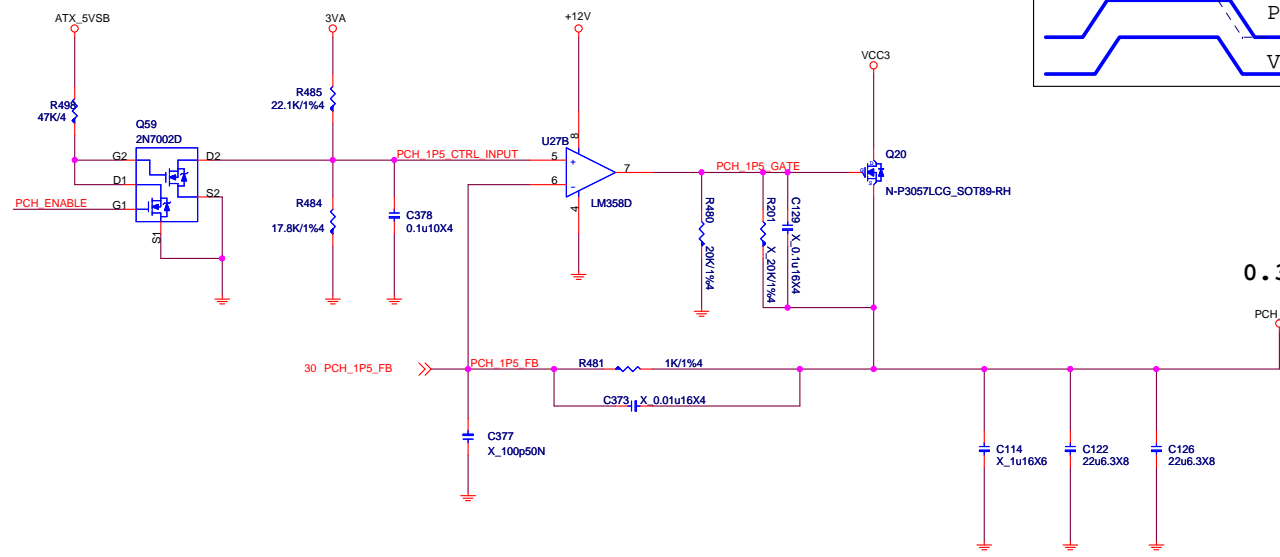
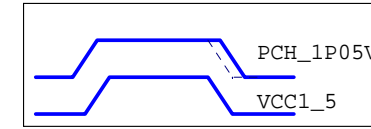
PCH: 0.35A

PCH\_1P5

Imax: 0.35A

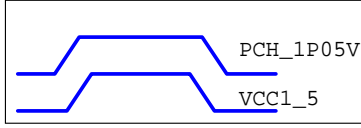
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VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



0.35A

VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH





7887\_1.0

PD0-0788710-G37,精成,23,寶安恩斯邁廠(MSIS)  
PD0-0788710-G37,精成,52,寶安恩斯邁廠(MSIS)  
PD0-0788710-E48,競華,23,寶安恩斯邁廠(MSIS)  
PD0-0788710-E48,競華,52,寶安恩斯邁廠(MSIS)

WIFI  
WIFI  
CADR  
WIFI\_CARD

LABEL2  
MKT  
X\_BUY

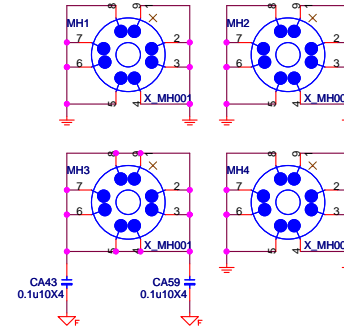
HDMI\_LA1  
Label  
BDW1  
HDMI\_LABEL

CPU\_H1  
CPU  
鐵座  
CPU\_H1

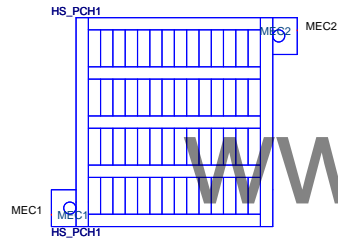
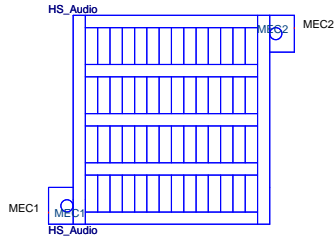
LA3  
AMT\_BIOS  
LABLE  
BIOS\_LABEL

BAT1\_X1  
BAT-BCR2032P-RH

## Mounting Holes

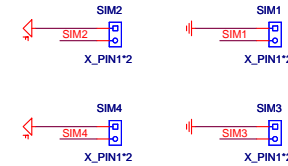


## HEATSINK

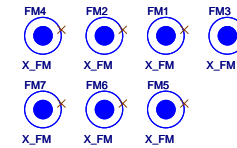


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## Simulation



## Optical Fiducial Marks-120



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	MS-7887		
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